

M16C/6N Group (M16C/6N4)

Renesas MCU

REJ03B0003-0240

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1. Overview

The M16C/6N Group (M16C/6N4) of MCUs are built using the high-performance silicon gate CMOS process using the M16C/60 Series CPU core and are packaged in 100-pin plastic molded QFP and LQFP. These MCUs operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. Being equipped with two CAN (Controller Area Network) modules in the M16C/6N Group (M16C/6N4), the MCU is suited to drive automotive and industrial control systems. The CAN modules comply with the 2.0B specification. In addition, this MCU contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

- Automotive, industrial control systems and other automobile, other (T/V-ver. product)
- Car audio and industrial control systems, other (Normal-ver. product)

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Overview

Table 1.1 lists the Functions and Specifications for M16C/6N Group (M16C/6N4).

Table 1.1 Functions and Specifications for M16C/6N Group (M16C/6N4)

| Item | | Specification | | |
|-------------------------------|------------------------------------|--|---|---|
| | | Normal-ver. | T/V-ver. | |
| CPU | Number of fundamental instructions | 91 instructions | | |
| | Minimum instruction execution time | 41.7 ns (f(BCLK) = 24 MHz, 1/1 prescaler, without software wait) | 50.0 ns (f(BCLK) = 20 MHz, 1/1 prescaler, without software wait) | |
| | Operating mode | Single-chip, memory expansion, and microprocessor modes | | |
| | Address space | 1 Mbyte | | |
| | Memory capacity | Refer to Table 1.2 Product Information | | |
| Peripheral Function | Ports | Input/Output: 87 pins, Input: 1 pin | | |
| | Multifunction timers | Timer A: 16 bits × 5 channels Timer B: 16 bits × 6 channels Three-phase motor control circuit | | |
| | Serial interfaces | 3 channels Clock synchronous, UART, I ² C-bus ⁽¹⁾ , IEBus ⁽²⁾ 1 channel Clock synchronous | | |
| | A/D converter | 10-bit A/D converter: 1 circuit, 26 channels | | |
| | D/A converter | 8 bits × 2 channels | | |
| | DMAC | 2 channels | | |
| | CRC calculation circuit | CRC-CCITT | | |
| | CAN module | 2 channels with 2.0B specification | | |
| | Watchdog timer | 15 bits × 1 channel (with prescaler) | | |
| | Interrupts | Internal: 31 sources, External: 9 sources Software: 4 sources, Priority levels: 7 levels | | |
| | Clock generation circuits | 4 circuits • Main clock oscillation circuit (*) • Sub clock oscillation circuit (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with on-chip feedback resistor | | |
| | Oscillation-stopped detector | Main clock oscillation stop and re-oscillation detection function | | |
| | Electrical Characteristics | Supply voltage | VCC = 3.0 to 5.5 V (f(BCLK) = 24 MHz, 1/1 prescaler, without software wait) | VCC = 4.2 to 5.5 V (f(BCLK) = 20 MHz, 1/1 prescaler, without software wait) |
| Consumption current | | Mask ROM | 20 mA (f(BCLK) = 24 MHz, PLL operation, no division) | 18 mA (f(BCLK) = 20 MHz, PLL operation, no division) |
| | | Flash memory | 22 mA (f(BCLK) = 24 MHz, PLL operation, no division) | 20 mA (f(BCLK) = 20 MHz, PLL operation, no division) |
| | | Mask ROM Flash memory | 0.8 μA (Stop mode, Topr = 25°C) | |
| Flash Memory Version | Programming and erasure voltage | 3.0 ± 0.3 V or 5.0 ± 0.5 V | 5.0 ± 0.5 V | |
| | Programming and erasure endurance | 100 times | | |
| I/O Characteristics | I/O withstand voltage | 5.0 V | | |
| | Output current | 5 mA | | |
| Operating Ambient Temperature | -40 to 85°C | T version: -40 to 85°C V version: -40 to 125°C (option) | | |
| Device Configuration | CMOS high-performance silicon gate | | | |
| Package | 100-pin molded-plastic QFP, LQFP | | | |

NOTES:

1. I²C-bus is a trademark of Koninklijke Philips Electronics N.V.
2. IEBus is a trademark of NEC Electronics Corporation.

option: All options are on request basis.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

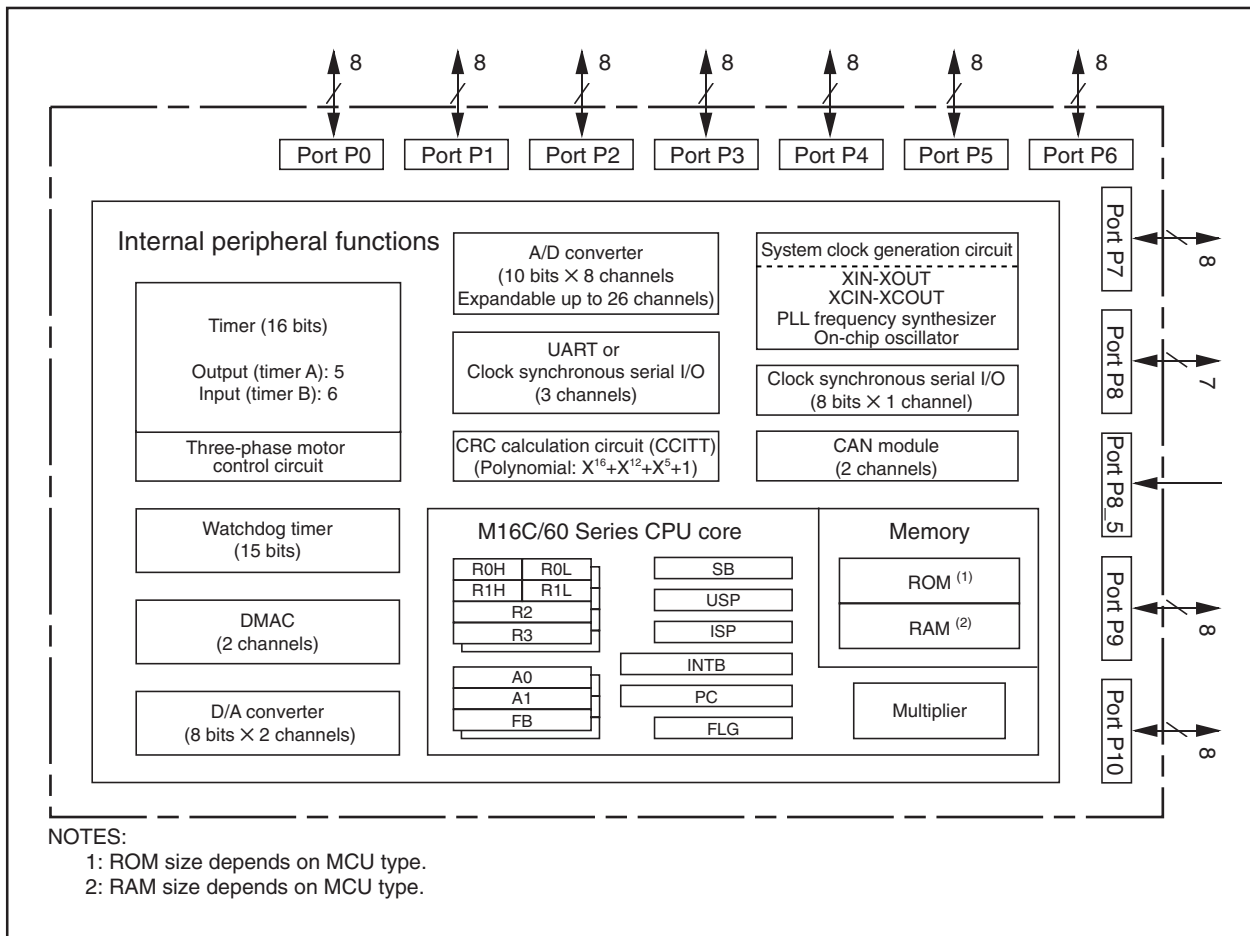


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the Product Information and Figure 1.2 shows the Type Number, Memory Size, and Packages.

Table 1.2 Product Information As of Aug. 2006

| Type No. | ROM Capacity | RAM Capacity | Package Type ⁽²⁾ | Remarks | | |
|---------------------|------------------|--------------|-----------------------------|-------------------------------------|-------------|-------------|
| M306N4FCFP | 128 K + 4 Kbytes | 5 Kbytes | PRQP0100JB-A | Flash memory version ⁽¹⁾ | Normal-ver. | |
| M306N4FCGP | | | PLQP0100KB-A | | | |
| M306N4FGFP | 256 K + 4 Kbytes | 10 Kbytes | PRQP0100JB-A | | | |
| M306N4FGGP | | | PLQP0100KB-A | | | |
| M306N4FCTFP | 128 K + 4 Kbytes | 5 Kbytes | PRQP0100JB-A | | | T-ver. |
| M306N4FCTGP | | | PLQP0100KB-A | | | |
| M306N4FGTFP | 256 K + 4 Kbytes | 10 Kbytes | PRQP0100JB-A | | | |
| M306N4FGTGP | | | PLQP0100KB-A | | | |
| M306N4FCVFP | 128 K + 4 Kbytes | 5 Kbytes | PRQP0100JB-A | | V-ver. | |
| M306N4FCVGP | | | PLQP0100KB-A | | | |
| M306N4FGVFP | 256 K + 4 Kbytes | 10 Kbytes | PRQP0100JB-A | | | |
| M306N4FGVGP | | | PLQP0100KB-A | | | |
| M306N4MC-XXXGP | 128 Kbytes | 5 Kbytes | PLQP0100KB-A | Mask ROM version | | Normal-ver. |
| M306N4MG-XXXGP | 256 Kbytes | 10 Kbytes | PLQP0100KB-A | | | |
| M306N4MCT-XXXFP | 128 Kbytes | 5 Kbytes | PRQP0100JB-A | | T-ver. | |
| M306N4MCT-XXXGP | | | PLQP0100KB-A | | | |
| M306N4MGT-XXXFP | 256 Kbytes | 10 Kbytes | PRQP0100JB-A | | | |
| M306N4MGT-XXXGP | | | PLQP0100KB-A | | | |
| M306N4MCV-XXXFP | 128 Kbytes | 5 Kbytes | PRQP0100JB-A | | | V-ver. |
| M306N4MCV-XXXGP (D) | | | PLQP0100KB-A | | | |
| M306N4MGV-XXXFP | 256 Kbytes | 10 Kbytes | PRQP0100JB-A | | | |
| M306N4MGV-XXXGP (D) | | | PLQP0100KB-A | | | |

(D): Under development

NOTES:

1. Data flash memory provides an additional 4 Kbytes of ROM capacity (block A).
2. The correspondence between new and old package types is as follows.

PRQP0100JB-A: 100P6S-A
 PLQP0100KB-A: 100P6Q-A

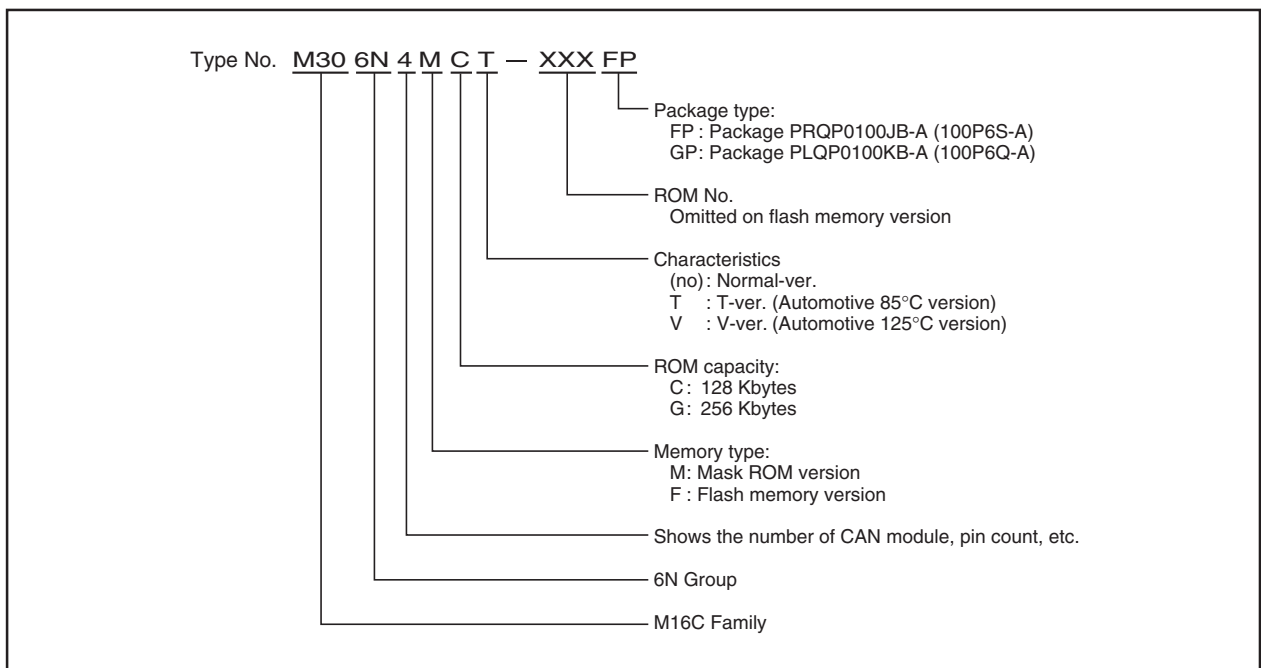


Figure 1.2 Type Number, Memory Size, and Package

1.5 Pin Assignments

Figures 1.3 and 1.4 show the Pin Assignment (Top View). Tables 1.3 and 1.4 list the List of Pin Names.

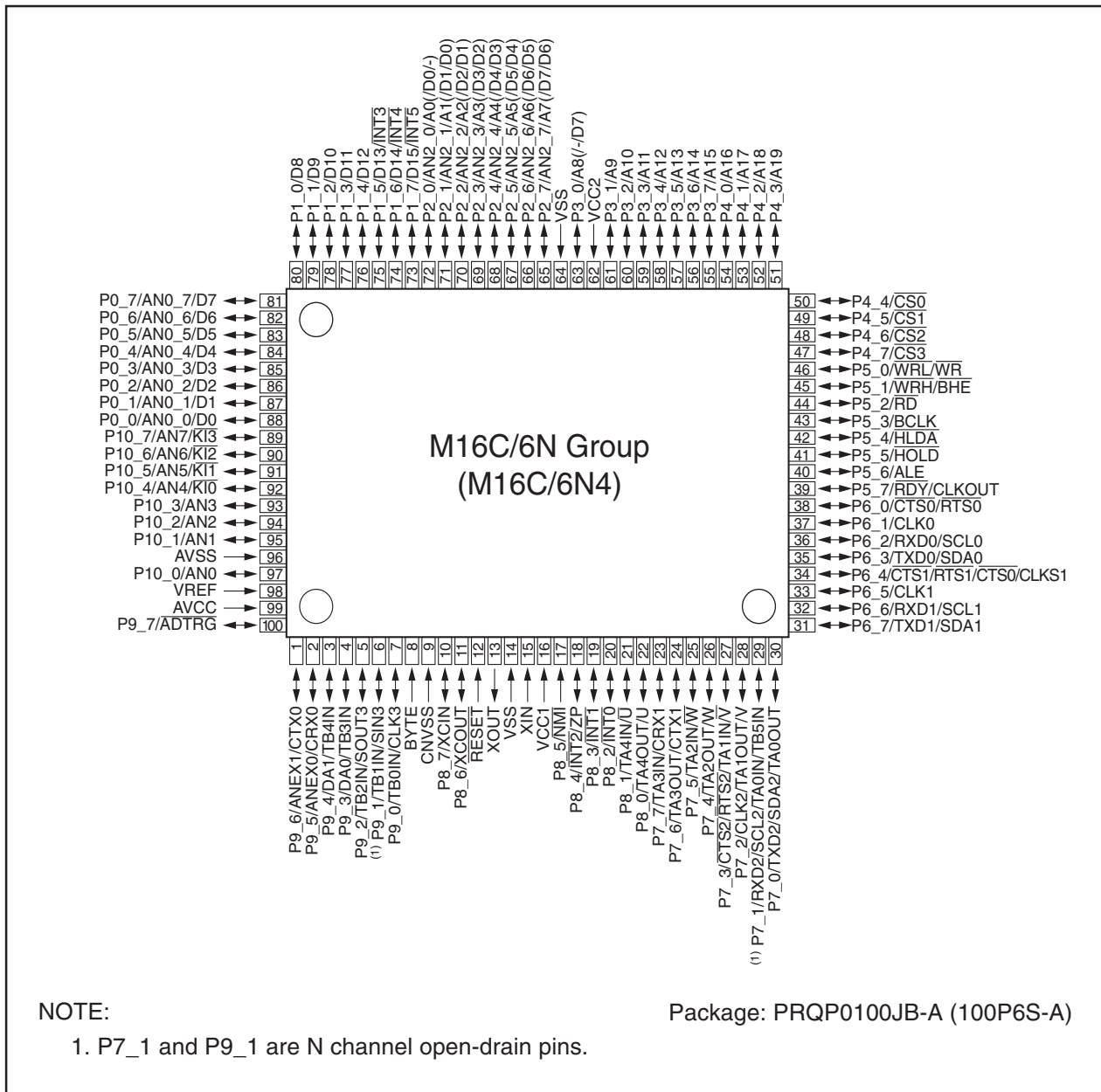


Figure 1.3 Pin Assignments (Top View) (1)

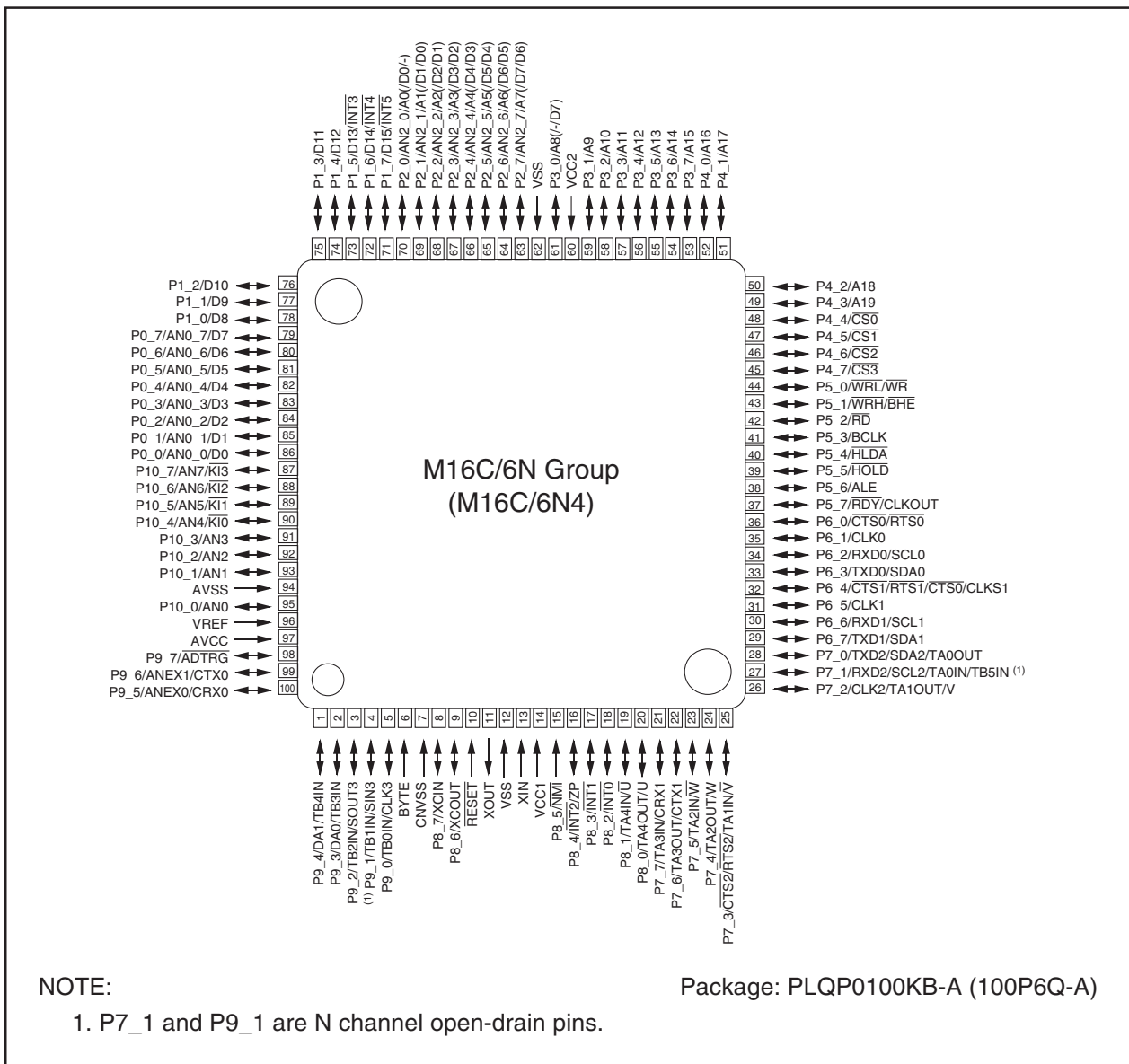


Table 1.3 List of Pin Names (1)

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | CAN Module Pin | Bus Control Pin |
|---------|-------------|-------|---------------|------------------|----------------------|------------|----------------|---------------------|
| FP | GP | | | | | | | |
| 1 | 99 | | P9_6 | | | ANEX1 | CTX0 | |
| 2 | 100 | | P9_5 | | | ANEX0 | CRX0 | |
| 3 | 1 | | P9_4 | TB4IN | | DA1 | | |
| 4 | 2 | | P9_3 | TB3IN | | DA0 | | |
| 5 | 3 | | P9_2 | TB2IN | SOUT3 | | | |
| 6 | 4 | | P9_1 | TB1IN | SIN3 | | | |
| 7 | 5 | | P9_0 | TB0IN | CLK3 | | | |
| 8 | 6 | BYTE | | | | | | |
| 9 | 7 | CNVSS | | | | | | |
| 10 | 8 | XCIN | P8_7 | | | | | |
| 11 | 9 | XCOU | P8_6 | | | | | |
| 12 | 10 | RESET | | | | | | |
| 13 | 11 | XOUT | | | | | | |
| 14 | 12 | VSS | | | | | | |
| 15 | 13 | XIN | | | | | | |
| 16 | 14 | VCC1 | | | | | | |
| 17 | 15 | | P8_5 | NMI | | | | |
| 18 | 16 | | P8_4 | INT2 | ZP | | | |
| 19 | 17 | | P8_3 | INT1 | | | | |
| 20 | 18 | | P8_2 | INT0 | | | | |
| 21 | 19 | | P8_1 | TA4IN/ \bar{U} | | | | |
| 22 | 20 | | P8_0 | TA4OUT/U | | | | |
| 23 | 21 | | P7_7 | TA3IN | | | CRX1 | |
| 24 | 22 | | P7_6 | TA3OUT | | | CTX1 | |
| 25 | 23 | | P7_5 | TA2IN/ \bar{W} | | | | |
| 26 | 24 | | P7_4 | TA2OUT/W | | | | |
| 27 | 25 | | P7_3 | TA1IN/ \bar{V} | CTS2/RTS2 | | | |
| 28 | 26 | | P7_2 | TA1OUT/V | CLK2 | | | |
| 29 | 27 | | P7_1 | TA0IN/TB5IN | RXD2/SCL2 | | | |
| 30 | 28 | | P7_0 | TA0OUT | TXD2/SDA2 | | | |
| 31 | 29 | | P6_7 | | TXD1/SDA1 | | | |
| 32 | 30 | | P6_6 | | RXD1/SCL1 | | | |
| 33 | 31 | | P6_5 | | CLK1 | | | |
| 34 | 32 | | P6_4 | | CTS1/RTS1/CTS0/CLKS1 | | | |
| 35 | 33 | | P6_3 | | TXD0/SDA0 | | | |
| 36 | 34 | | P6_2 | | RXD0/SCL0 | | | |
| 37 | 35 | | P6_1 | | CLK0 | | | |
| 38 | 36 | | P6_0 | | CTS0/RTS0 | | | |
| 39 | 37 | | P5_7 | | | | | \bar{RDY} /CLKOUT |
| 40 | 38 | | P5_6 | | | | | ALE |
| 41 | 39 | | P5_5 | | | | | HOLD |
| 42 | 40 | | P5_4 | | | | | HLDA |
| 43 | 41 | | P5_3 | | | | | BCLK |
| 44 | 42 | | P5_2 | | | | | \bar{RD} |
| 45 | 43 | | P5_1 | | | | | WRH/BHE |
| 46 | 44 | | P5_0 | | | | | WRL/WR |
| 47 | 45 | | P4_7 | | | | | CS3 |
| 48 | 46 | | P4_6 | | | | | CS2 |
| 49 | 47 | | P4_5 | | | | | CS1 |
| 50 | 48 | | P4_4 | | | | | CS0 |

FP: PRQP0100JB-A (100P6S-A), GP: PLQP0100KB-A (100P6Q-A)

Table 1.4 List of Pin Names (2)

| Pin No. | | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | CAN Module Pin | Bus Control Pin |
|---------|----|-------------|-------|---------------|-----------|----------|------------|----------------|-----------------|
| FP | GP | | | | | | | | |
| 51 | 49 | | P4_3 | | | | | | A19 |
| 52 | 50 | | P4_2 | | | | | | A18 |
| 53 | 51 | | P4_1 | | | | | | A17 |
| 54 | 52 | | P4_0 | | | | | | A16 |
| 55 | 53 | | P3_7 | | | | | | A15 |
| 56 | 54 | | P3_6 | | | | | | A14 |
| 57 | 55 | | P3_5 | | | | | | A13 |
| 58 | 56 | | P3_4 | | | | | | A12 |
| 59 | 57 | | P3_3 | | | | | | A11 |
| 60 | 58 | | P3_2 | | | | | | A10 |
| 61 | 59 | | P3_1 | | | | | | A9 |
| 62 | 60 | VCC2 | | | | | | | |
| 63 | 61 | | P3_0 | | | | | | A8(/-/D7) |
| 64 | 62 | VSS | | | | | | | |
| 65 | 63 | | P2_7 | | | | AN2_7 | | A7(/D7/D6) |
| 66 | 64 | | P2_6 | | | | AN2_6 | | A6(/D6/D5) |
| 67 | 65 | | P2_5 | | | | AN2_5 | | A5(/D5/D4) |
| 68 | 66 | | P2_4 | | | | AN2_4 | | A4(/D4/D3) |
| 69 | 67 | | P2_3 | | | | AN2_3 | | A3(/D3/D2) |
| 70 | 68 | | P2_2 | | | | AN2_2 | | A2(/D2/D1) |
| 71 | 69 | | P2_1 | | | | AN2_1 | | A1(/D1/D0) |
| 72 | 70 | | P2_0 | | | | AN2_0 | | A0(/D0/-) |
| 73 | 71 | | P1_7 | INT5 | | | | | D15 |
| 74 | 72 | | P1_6 | INT4 | | | | | D14 |
| 75 | 73 | | P1_5 | INT3 | | | | | D13 |
| 76 | 74 | | P1_4 | | | | | | D12 |
| 77 | 75 | | P1_3 | | | | | | D11 |
| 78 | 76 | | P1_2 | | | | | | D10 |
| 79 | 77 | | P1_1 | | | | | | D9 |
| 80 | 78 | | P1_0 | | | | | | D8 |
| 81 | 79 | | P0_7 | | | | AN0_7 | | D7 |
| 82 | 80 | | P0_6 | | | | AN0_6 | | D6 |
| 83 | 81 | | P0_5 | | | | AN0_5 | | D5 |
| 84 | 82 | | P0_4 | | | | AN0_4 | | D4 |
| 85 | 83 | | P0_3 | | | | AN0_3 | | D3 |
| 86 | 84 | | P0_2 | | | | AN0_2 | | D2 |
| 87 | 85 | | P0_1 | | | | AN0_1 | | D1 |
| 88 | 86 | | P0_0 | | | | AN0_0 | | D0 |
| 89 | 87 | | P10_7 | KI3 | | | AN7 | | |
| 90 | 88 | | P10_6 | KI2 | | | AN6 | | |
| 91 | 89 | | P10_5 | KI1 | | | AN5 | | |
| 92 | 90 | | P10_4 | KI0 | | | AN4 | | |
| 93 | 91 | | P10_3 | | | | AN3 | | |
| 94 | 92 | | P10_2 | | | | AN2 | | |
| 95 | 93 | | P10_1 | | | | AN1 | | |
| 96 | 94 | AVSS | | | | | | | |
| 97 | 95 | | P10_0 | | | | AN0 | | |
| 98 | 96 | VREF | | | | | | | |
| 99 | 97 | AVCC | | | | | | | |
| 100 | 98 | | P9_7 | | | | ADTRG | | |

FP: PRQP0100JB-A (100P6S-A), GP: PLQP0100KB-A (100P6Q-A)

1.6 Pin Functions

Tables 1.5 to 1.7 list the Pin Functions.

Table 1.5 Pin Functions (1)

| Signal Name | Pin Name | I/O Type | Description |
|--------------------------------------|-------------------------|--|---|
| Power supply input | VCC1, VCC2, VSS | I | Apply 4.2 to 5.5 V (T/V-ver.), 3.0 to 5.5 V (Normal-ver.) to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC2 = VCC1 ⁽¹⁾ . |
| Analog power supply input | AVCC, AVSS | I | Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS. |
| Reset input | RESET | I | The MCU is in a reset state when applying "L" to the this pin. |
| CNVSS | CNVSS | I | Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. |
| External data bus width select input | BYTE | I | Switches the data bus in external memory space. The data bus is 16-bit long when the this pin is held "L" and 8-bit long when the this pin is held "H". Set it to either one. Connect this pin to VSS when single-chip mode. |
| Bus control pins | D0 to D7 | I/O | Inputs and outputs data (D0 to D7) when these pins are set as the separate bus. |
| | D8 to D15 | I/O | Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus. |
| | A0 to A19 | O | Output address bits (A0 to A19). |
| | A0/D0 to A7/D7 | I/O | Input and output data (D0 to D7) and output address bits (A0 to A7) by time-sharing when external 8-bit data bus are set as the multiplexed bus. |
| | A1/D0 to A8/D7 | I/O | Input and output data (D0 to D7) and output address bits (A1 to A8) by time-sharing when external 16-bit data bus are set as the multiplexed bus. |
| | CS0 to CS3 | O | Output CS0 to CS3 signals. CS0 to CS3 are chip-select signals to specify an external space. |
| | WRL/WR WRH/BHE RD | O | Output WRL, WRH, (WR, BHE), RD signals. WRL and WRH or BHE, and WR can be switched by program. <ul style="list-style-type: none"> • WRL, WRH, and RD are selected The WRL signal becomes "L" by writing data to an even address in an external memory space. The WRH signal becomes "L" by writing data to an odd address in an external memory space. The RD pin signal becomes "L" by reading data in an external memory space. • WR, BHE, and RD are selected The WR signal becomes "L" by writing data in an external memory space. The RD signal becomes "L" by reading data in an external memory space. The BHE signal becomes "L" by accessing an odd address. Select WR, BHE, and RD for an external 8-bit data bus. |
| | ALE | O | ALE is a signal to latch the address. |
| | HOLD | I | While the HOLD pin is held "L", the MCU is placed in a hold state. |
| | HLDA | O | In a hold state, HLDA outputs a "L" signal. |
| RDY | I | While applying a "L" signal to the RDY pin, the MCU is placed in a wait state. | |

I: Input O: Output I/O: Input/Output

NOTE:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.

Table 1.6 Pin Functions (2)

| Signal Name | Pin Name | I/O Type | Description |
|----------------------------------|--|----------|--|
| Main clock input | XIN | I | I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT ⁽¹⁾ . |
| Main clock output | XOUT | O | To use the external clock, input the clock from XIN and leave XOUT open. |
| Sub clock input | XCIN | I | I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOU ⁽¹⁾ . |
| Sub clock output | XCOU | O | To use the external clock, input the clock from XCIN and leave XCOU open. |
| BCLK output | BCLK | O | Outputs the BCLK signal. |
| Clock output | CLKOUT | O | The clock of the same cycle as fC, f8, or f32 is output. |
| INT interrupt input | INT0 to INT5 | I | Input pins for the INT interrupt. |
| NMI interrupt input | NMI | I | Input pin for the NMI interrupt. |
| Key input interrupt input | KI0 to KI3 | I | Input pins for the key input interrupt. |
| Timer A | TA0OUT to TA4OUT | I/O | These are timer A0 to timer A4 I/O pins. |
| | TA0IN to TA4IN | I | These are timer A0 to timer A4 input pins. |
| | ZP | I | Input pin for the Z-phase. |
| Timer B | TB0IN to TB5IN | I | These are timer B0 to timer B5 input pins. |
| Three-phase motor control output | U, U, V, V, W, W | O | These are Three-phase motor control output pins. |
| Serial interface | CTS0 to CTS2 | I | These are transmit control input pins. |
| | RTS0 to RTS2 | O | These are receive control output pins. |
| | CLK0 to CLK3 | I/O | These are transfer clock I/O pins. |
| | RXD0 to RXD2 | I | These are serial data input pins. |
| | SIN3 | I | These are serial data input pins. |
| | TXD0 to TXD2 | O | These are serial data output pins. |
| | SOUT3 | O | These are serial data output pins. |
| | CLKS1 | O | This is output pin for transfer clock output from multiple pins function. |
| I ² C mode | SDA0 to SDA2 | I/O | These are serial data I/O pins. |
| | SCL0 to SCL2 | I/O | These are transfer clock I/O pins. (however, SCL2 for the N-channel open drain output.) |
| Reference voltage input | VREF | I | Applies the reference voltage for the A/D converter and D/A converter. |
| A/D converter | AN0 to AN7 AN0_0 to AN0_7 AN2_0 to AN2_7 | I | Analog input pins for the A/D converter. |
| | ADTRG | I | This is an A/D trigger input pin. |
| | ANEX0 | I/O | This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode. |
| | ANEX1 | I | This is the extended analog input pin for the A/D converter. |
| D/A converter | DA0, DA1 | O | These are the output pins for the D/A converter. |
| CAN module | CRX0, CRX1 | I | These are the input pins for the CAN module. |
| | CTX0, CTX1 | O | These are the output pins for the CAN module. |

I: Input O: Output I/O: Input/Output

NOTE:

1. Ask the oscillator maker the oscillation characteristic.

Table 1.7 Pin Functions (3)

| Signal Name | Pin Name | I/O Type | Description |
|-------------|--|----------|--|
| I/O port | P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7 P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_4 P8_6, P8_7 P9_0 to P9_7 P10_0 to P10_7 | I/O | 8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. (however, P7_1 and P9_1 for the N-channel open drain output.) |
| Input port | P8_5 | I | Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register. |

I: Input O: Output I/O: Input/Output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two register banks.

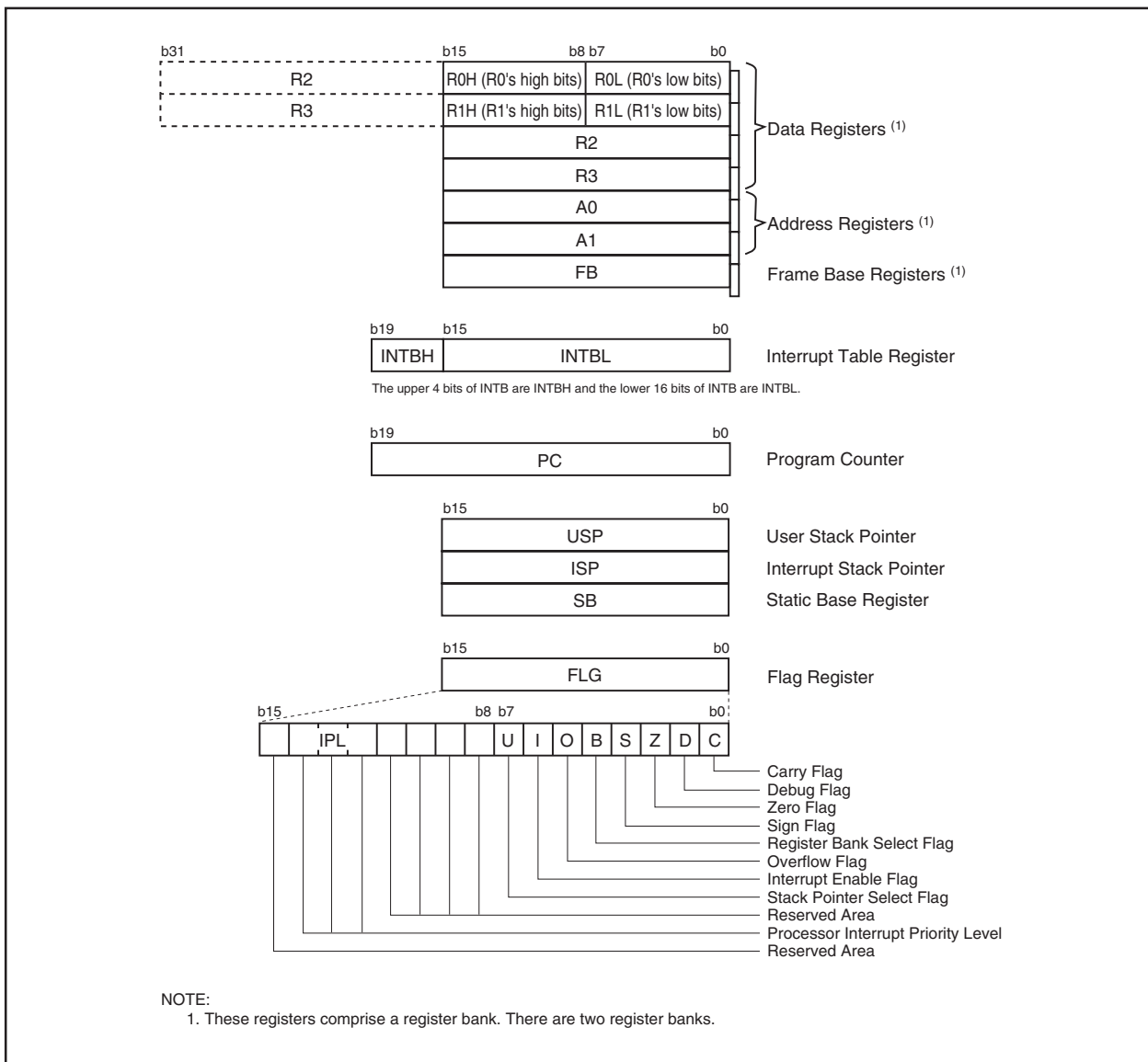


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits. Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is set to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

3. Memory

Figure 3.1 shows a Memory Map. The address space extends the 1 Mbyte from address 00000h to FFFFFh. The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 128-Kbyte internal ROM is allocated to the addresses from E0000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400h to 017FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The Special Function Registers (SFRs) are allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be accessed by user.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to **M16C/60, M16C/20, M16C/Tiny Series Software Manual**.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.

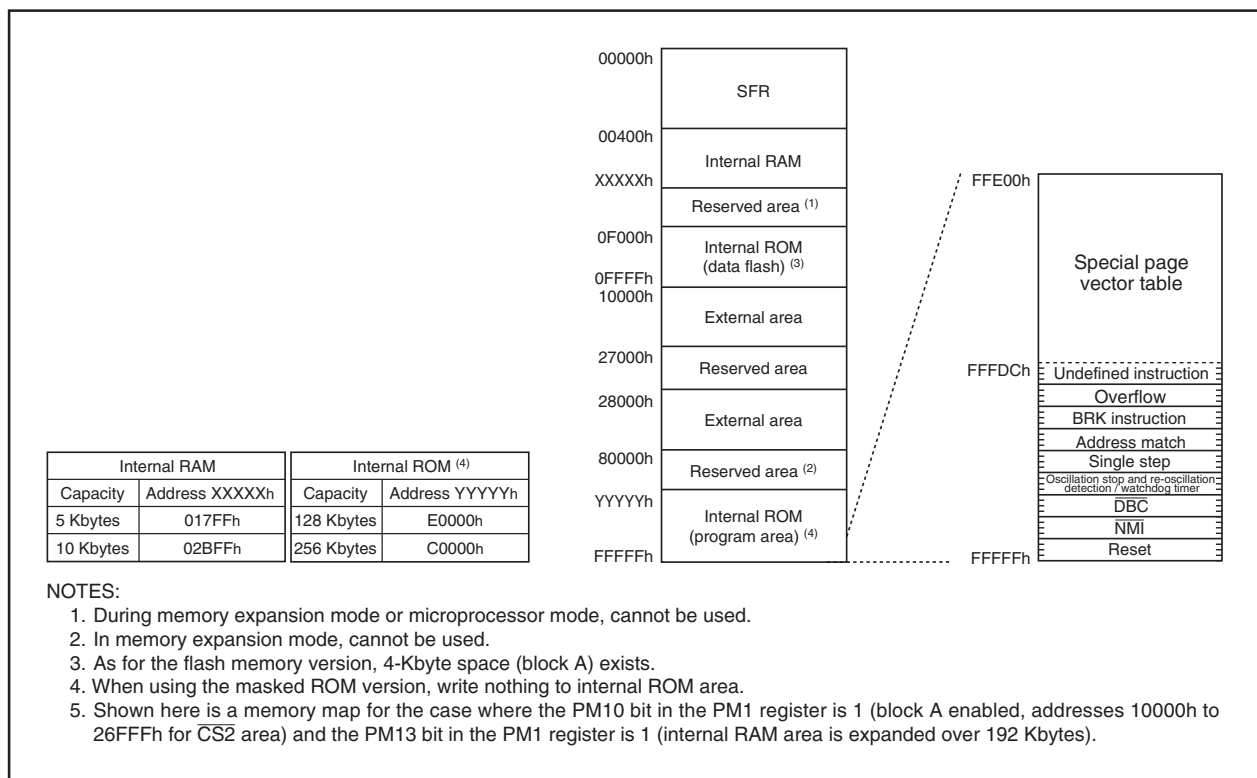


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

An SFR (Special Function Register) is a control register for a peripheral function.

Tables 4.1 to 4.16 list the SFR Information.

Table 4.1 SFR Information (1) ⁽³⁾

| Address | Register | Symbol | After Reset |
|---------|--|--------|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 ⁽¹⁾ | PM0 | 0000000b (CNVSS pin is "L") 00000011b (CNVSS pin is "H") |
| 0005h | Processor Mode Register 1 | PM1 | 00001000b |
| 0006h | System Clock Control Register 0 | CM0 | 01001000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Chip Select Control Register | CSR | 00000001b |
| 0009h | Address Match Interrupt Enable Register | AIER | XXXXXX00b |
| 000Ah | Protect Register | PRCR | XX000000b |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register ⁽²⁾ | CM2 | 0X000000b |
| 000Dh | | | |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00XXXXXXb |
| 0010h | | | 00h |
| 0011h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0012h | | | X0h |
| 0013h | | | |
| 0014h | | | 00h |
| 0015h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0016h | | | X0h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | Chip Select Expansion Control Register | CSE | 00h |
| 001Ch | PLL Control Register 0 | PLC0 | 0001X010b |
| 001Dh | | | |
| 001Eh | Processor Mode Register 2 | PM2 | XXX00000b |
| 001Fh | | | |
| 0020h | | | XXh |
| 0021h | DMA0 Source Pointer | SAR0 | XXh |
| 0022h | | | XXh |
| 0023h | | | |
| 0024h | | | XXh |
| 0025h | DMA0 Destination Pointer | DAR0 | XXh |
| 0026h | | | XXh |
| 0027h | | | |
| 0028h | DMA0 Transfer Counter | TCR0 | XXh |
| 0029h | | | XXh |
| 002Ah | | | |
| 002Bh | | | |
| 002Ch | DMA0 Control Register | DM0CON | 00000X00b |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |
| 0030h | | | XXh |
| 0031h | DMA1 Source Pointer | SAR1 | XXh |
| 0032h | | | XXh |
| 0033h | | | |
| 0034h | | | XXh |
| 0035h | DMA1 Destination Pointer | DAR1 | XXh |
| 0036h | | | XXh |
| 0037h | | | |
| 0038h | DMA1 Transfer Counter | TCR1 | XXh |
| 0039h | | | XXh |
| 003Ah | | | |
| 003Bh | | | |
| 003Ch | DMA1 Control Register | DM1CON | 00000X00b |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |

X: Undefined

NOTES:

1. Bits PM00 and PM01 in the PM0 register do not change at software reset, watchdog timer reset and oscillation stop detection reset.
2. Bits CM20, CM21, and CM27 in the CM2 register do not change at oscillation stop detection reset.
3. Blank spaces are reserved. No access is allowed.

Table 4.2 SFR Information (2) ⁽¹⁾

| Address | Register | Symbol | After Reset |
|---------|--|----------|-------------|
| 0040h | | | |
| 0041h | CAN0/1 Wake-up Interrupt Control Register | C01WKIC | XXXXX000b |
| 0042h | CAN0 Successful Reception Interrupt Control Register | C0RECIC | XXXXX000b |
| 0043h | CAN0 Successful Transmission Interrupt Control Register | C0TRMIC | XXXXX000b |
| 0044h | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 0045h | Timer B5 Interrupt Control Register | TB5IC | XXXXX000b |
| 0046h | Timer B4 Interrupt Control Register | TB4IC | XXXXX000b |
| | UART1 Bus Collision Detection Interrupt Control Register | U1BCNIC | |
| 0047h | Timer B3 Interrupt Control Register | TB3IC | XXXXX000b |
| | UART0 Bus Collision Detection Interrupt Control Register | U0BCNIC | |
| 0048h | CAN1 Successful Reception Interrupt Control Register | C1RECIC | XX00X000b |
| | INT5 Interrupt Control Register | INT5IC | |
| 0049h | CAN1 Successful Transmission Interrupt Control Register | C1TRMIC | XX00X000b |
| | SI/O3 Interrupt Control Register | S3IC | |
| | INT4 Interrupt Control Register | INT4IC | |
| 004Ah | UART2 Bus Collision Detection Interrupt Control Register | U2BCNIC | XXXXX000b |
| 004Bh | DMA0 Interrupt Control Register | DM0IC | XXXXX000b |
| 004Ch | DMA1 Interrupt Control Register | DM1IC | XXXXX000b |
| 004Dh | CAN0/1 Error Interrupt Control Register | C01ERRIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| | Key Input Interrupt Control Register | KUPIC | |
| 004Fh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 0050h | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | Timer A0 Interrupt Control Register | TA0IC | XXXXX000b |
| 0056h | Timer A1 Interrupt Control Register | TA1IC | XXXXX000b |
| 0057h | Timer A2 Interrupt Control Register | TA2IC | XXXXX000b |
| 0058h | Timer A3 Interrupt Control Register | TA3IC | XXXXX000b |
| 0059h | Timer A4 Interrupt Control Register | TA4IC | XXXXX000b |
| 005Ah | Timer B0 Interrupt Control Register | TB0IC | XXXXX000b |
| 005Bh | Timer B1 Interrupt Control Register | TB1IC | XXXXX000b |
| 005Ch | Timer B2 Interrupt Control Register | TB2IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Fh | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0060h | | | XXh |
| 0061h | | | XXh |
| 0062h | CAN0 Message Box 0: Identifier / DLC | | XXh |
| 0063h | | | XXh |
| 0064h | | | XXh |
| 0065h | | | XXh |
| 0066h | | | XXh |
| 0067h | CAN0 Message Box 0: Data Field | | XXh |
| 0068h | | | XXh |
| 0069h | | | XXh |
| 006Ah | | | XXh |
| 006Bh | | | XXh |
| 006Ch | | | XXh |
| 006Dh | | | XXh |
| 006Eh | CAN0 Message Box 0: Time Stamp | | XXh |
| 006Fh | | | XXh |
| 0070h | | | XXh |
| 0071h | CAN0 Message Box 1: Identifier / DLC | | XXh |
| 0072h | | | XXh |
| 0073h | | | XXh |
| 0074h | | | XXh |
| 0075h | | | XXh |
| 0076h | CAN0 Message Box 1: Data Field | | XXh |
| 0077h | | | XXh |
| 0078h | | | XXh |
| 0079h | | | XXh |
| 007Ah | | | XXh |
| 007Bh | | | XXh |
| 007Ch | | | XXh |
| 007Dh | | XXh | |
| 007Eh | CAN0 Message Box 1: Time Stamp | | XXh |
| 007Fh | | | XXh |

X: Undefined

NOTE:

- Blank space is reserved. No access is allowed.

Table 4.3 SFR Information (3)

| Address | Register | Symbol | After Reset | | |
|---------|--------------------------------------|--------|--------------------------------------|--|-----|
| 0080h | CAN0 Message Box 2: Identifier / DLC | | XXh | | |
| 0081h | | | XXh | | |
| 0082h | | | XXh | | |
| 0083h | | | XXh | | |
| 0084h | | | XXh | | |
| 0085h | | | XXh | | |
| 0086h | CAN0 Message Box 2: Data Field | | XXh | | |
| 0087h | | | XXh | | |
| 0088h | | | XXh | | |
| 0089h | | | XXh | | |
| 008Ah | | | XXh | | |
| 008Bh | | | XXh | | |
| 008Ch | CAN0 Message Box 2: Time Stamp | | XXh | | |
| 008Dh | | | XXh | | |
| 008Eh | | | XXh | | |
| 008Fh | | | XXh | | |
| 0090h | | | CAN0 Message Box 3: Identifier / DLC | | XXh |
| 0091h | | | | | XXh |
| 0092h | XXh | | | | |
| 0093h | XXh | | | | |
| 0094h | XXh | | | | |
| 0095h | XXh | | | | |
| 0096h | CAN0 Message Box 3: Data Field | | XXh | | |
| 0097h | | | XXh | | |
| 0098h | | | XXh | | |
| 0099h | | | XXh | | |
| 009Ah | | | XXh | | |
| 009Bh | | | XXh | | |
| 009Ch | CAN0 Message Box 3: Time Stamp | | XXh | | |
| 009Dh | | | XXh | | |
| 009Eh | | | XXh | | |
| 009Fh | | | XXh | | |
| 00A0h | | | CAN0 Message Box 4: Identifier / DLC | | XXh |
| 00A1h | | | | | XXh |
| 00A2h | XXh | | | | |
| 00A3h | XXh | | | | |
| 00A4h | XXh | | | | |
| 00A5h | XXh | | | | |
| 00A6h | CAN0 Message Box 4: Data Field | | XXh | | |
| 00A7h | | | XXh | | |
| 00A8h | | | XXh | | |
| 00A9h | | | XXh | | |
| 00AAh | | | XXh | | |
| 00ABh | | | XXh | | |
| 00ACh | CAN0 Message Box 4: Time Stamp | | XXh | | |
| 00ADh | | | XXh | | |
| 00AEh | | | XXh | | |
| 00AFh | | | XXh | | |
| 00B0h | | | CAN0 Message Box 5: Identifier / DLC | | XXh |
| 00B1h | | | | | XXh |
| 00B2h | XXh | | | | |
| 00B3h | XXh | | | | |
| 00B4h | XXh | | | | |
| 00B5h | XXh | | | | |
| 00B6h | CAN0 Message Box 5: Data Field | | XXh | | |
| 00B7h | | | XXh | | |
| 00B8h | | | XXh | | |
| 00B9h | | | XXh | | |
| 00BAh | | | XXh | | |
| 00BBh | | | XXh | | |
| 00BCh | CAN0 Message Box 5: Time Stamp | | XXh | | |
| 00BDh | | | XXh | | |
| 00BEh | | | XXh | | |
| 00BFh | | | XXh | | |

X: Undefined

Table 4.4 SFR Information (4)

| Address | Register | Symbol | After Reset | | |
|---------|--------------------------------------|--------|--------------------------------------|--|-----|
| 00C0h | CAN0 Message Box 6: Identifier / DLC | | XXh | | |
| 00C1h | | | XXh | | |
| 00C2h | | | XXh | | |
| 00C3h | | | XXh | | |
| 00C4h | | | XXh | | |
| 00C5h | | | XXh | | |
| 00C6h | CAN0 Message Box 6: Data Field | | XXh | | |
| 00C7h | | | XXh | | |
| 00C8h | | | XXh | | |
| 00C9h | | | XXh | | |
| 00CAh | | | XXh | | |
| 00CBh | | | XXh | | |
| 00CCh | CAN0 Message Box 6: Time Stamp | | XXh | | |
| 00CDh | | | XXh | | |
| 00CEh | | | XXh | | |
| 00CFh | | | XXh | | |
| 00D0h | | | CAN0 Message Box 7: Identifier / DLC | | XXh |
| 00D1h | | | | | XXh |
| 00D2h | XXh | | | | |
| 00D3h | XXh | | | | |
| 00D4h | XXh | | | | |
| 00D5h | XXh | | | | |
| 00D6h | CAN0 Message Box 7: Data Field | | XXh | | |
| 00D7h | | | XXh | | |
| 00D8h | | | XXh | | |
| 00D9h | | | XXh | | |
| 00DAh | | | XXh | | |
| 00DBh | | | XXh | | |
| 00DCh | CAN0 Message Box 7: Time Stamp | | XXh | | |
| 00DDh | | | XXh | | |
| 00DEh | | | XXh | | |
| 00DFh | | | XXh | | |
| 00E0h | | | CAN0 Message Box 8: Identifier / DLC | | XXh |
| 00E1h | | | | | XXh |
| 00E2h | XXh | | | | |
| 00E3h | XXh | | | | |
| 00E4h | XXh | | | | |
| 00E5h | XXh | | | | |
| 00E6h | CAN0 Message Box 8: Data Field | | XXh | | |
| 00E7h | | | XXh | | |
| 00E8h | | | XXh | | |
| 00E9h | | | XXh | | |
| 00EAh | | | XXh | | |
| 00EBh | | | XXh | | |
| 00ECh | CAN0 Message Box 8: Time Stamp | | XXh | | |
| 00EDh | | | XXh | | |
| 00EEh | | | XXh | | |
| 00EFh | | | XXh | | |
| 00F0h | | | CAN0 Message Box 9: Identifier / DLC | | XXh |
| 00F1h | | | | | XXh |
| 00F2h | XXh | | | | |
| 00F3h | XXh | | | | |
| 00F4h | XXh | | | | |
| 00F5h | XXh | | | | |
| 00F6h | CAN0 Message Box 9: Data Field | | XXh | | |
| 00F7h | | | XXh | | |
| 00F8h | | | XXh | | |
| 00F9h | | | XXh | | |
| 00FAh | | | XXh | | |
| 00FBh | | | XXh | | |
| 00FCh | CAN0 Message Box 9: Time Stamp | | XXh | | |
| 00FDh | | | XXh | | |
| 00FEh | | | XXh | | |
| 00FFh | | | XXh | | |

X: Undefined

Table 4.5 SFR Information (5)

| Address | Register | Symbol | After Reset | | |
|---------|---------------------------------------|--------|---------------------------------------|--|-----|
| 0100h | CAN0 Message Box 10: Identifier / DLC | | XXh | | |
| 0101h | | | XXh | | |
| 0102h | | | XXh | | |
| 0103h | | | XXh | | |
| 0104h | | | XXh | | |
| 0105h | | | XXh | | |
| 0106h | CAN0 Message Box 10: Data Field | | XXh | | |
| 0107h | | | XXh | | |
| 0108h | | | XXh | | |
| 0109h | | | XXh | | |
| 010Ah | | | XXh | | |
| 010Bh | | | XXh | | |
| 010Ch | CAN0 Message Box 10: Time Stamp | | XXh | | |
| 010Dh | | | XXh | | |
| 010Eh | | | XXh | | |
| 010Fh | | | XXh | | |
| 0110h | | | CAN0 Message Box 11: Identifier / DLC | | XXh |
| 0111h | | | | | XXh |
| 0112h | XXh | | | | |
| 0113h | XXh | | | | |
| 0114h | XXh | | | | |
| 0115h | XXh | | | | |
| 0116h | CAN0 Message Box 11: Data Field | | XXh | | |
| 0117h | | | XXh | | |
| 0118h | | | XXh | | |
| 0119h | | | XXh | | |
| 011Ah | | | XXh | | |
| 011Bh | | | XXh | | |
| 011Ch | CAN0 Message Box 11: Time Stamp | | XXh | | |
| 011Dh | | | XXh | | |
| 011Eh | | | XXh | | |
| 011Fh | | | XXh | | |
| 0120h | | | CAN0 Message Box 12: Identifier / DLC | | XXh |
| 0121h | | | | | XXh |
| 0122h | XXh | | | | |
| 0123h | XXh | | | | |
| 0124h | XXh | | | | |
| 0125h | XXh | | | | |
| 0126h | CAN0 Message Box 12: Data Field | | XXh | | |
| 0127h | | | XXh | | |
| 0128h | | | XXh | | |
| 0129h | | | XXh | | |
| 012Ah | | | XXh | | |
| 012Bh | | | XXh | | |
| 012Ch | CAN0 Message Box 12: Time Stamp | | XXh | | |
| 012Dh | | | XXh | | |
| 012Eh | | | XXh | | |
| 012Fh | | | XXh | | |
| 0130h | | | CAN0 Message Box 13: Identifier / DLC | | XXh |
| 0131h | | | | | XXh |
| 0132h | XXh | | | | |
| 0133h | XXh | | | | |
| 0134h | XXh | | | | |
| 0135h | XXh | | | | |
| 0136h | CAN0 Message Box 13: Data Field | | XXh | | |
| 0137h | | | XXh | | |
| 0138h | | | XXh | | |
| 0139h | | | XXh | | |
| 013Ah | | | XXh | | |
| 013Bh | | | XXh | | |
| 013Ch | CAN0 Message Box 13: Time Stamp | | XXh | | |
| 013Dh | | | XXh | | |
| 013Eh | | | XXh | | |
| 013Fh | | | XXh | | |

X: Undefined

Table 4.6 SFR Information (6) ⁽¹⁾

| Address | Register | Symbol | After Reset | | |
|---------|--------------------------------------|--------|--------------------------------------|-------|-----|
| 0140h | CAN0 Message Box 14: Identifier /DLC | | XXh | | |
| 0141h | | | XXh | | |
| 0142h | | | XXh | | |
| 0143h | | | XXh | | |
| 0144h | | | XXh | | |
| 0145h | | | XXh | | |
| 0146h | CAN0 Message Box 14: Data Field | | XXh | | |
| 0147h | | | XXh | | |
| 0148h | | | XXh | | |
| 0149h | | | XXh | | |
| 014Ah | | | XXh | | |
| 014Bh | | | XXh | | |
| 014Ch | CAN0 Message Box 14: Time Stamp | | XXh | | |
| 014Dh | | | XXh | | |
| 014Eh | | | XXh | | |
| 014Fh | | | XXh | | |
| 0150h | | | CAN0 Message Box 15: Identifier /DLC | | XXh |
| 0151h | | | | | XXh |
| 0152h | XXh | | | | |
| 0153h | XXh | | | | |
| 0154h | XXh | | | | |
| 0155h | XXh | | | | |
| 0156h | CAN0 Message Box 15: Data Field | | XXh | | |
| 0157h | | | XXh | | |
| 0158h | | | XXh | | |
| 0159h | | | XXh | | |
| 015Ah | | | XXh | | |
| 015Bh | | | XXh | | |
| 015Ch | CAN0 Message Box 15: Time Stamp | | XXh | | |
| 015Dh | | | XXh | | |
| 015Eh | | | XXh | | |
| 015Fh | | | XXh | | |
| 0160h | | | CAN0 Global Mask Register | C0GMR | XXh |
| 0161h | | | | | XXh |
| 0162h | XXh | | | | |
| 0163h | XXh | | | | |
| 0164h | XXh | | | | |
| 0165h | XXh | | | | |
| 0166h | CAN0 Local Mask A Register | C0LMAR | XXh | | |
| 0167h | | | XXh | | |
| 0168h | | | XXh | | |
| 0169h | | | XXh | | |
| 016Ah | | | XXh | | |
| 016Bh | | | XXh | | |
| 016Ch | CAN0 Local Mask B Register | C0LMBR | XXh | | |
| 016Dh | | | XXh | | |
| 016Eh | | | XXh | | |
| 016Fh | | | XXh | | |
| 0170h | | | XXh | | |
| 0171h | | | XXh | | |
| 0172h | | | | | |
| 0173h | | | | | |
| 0174h | | | | | |
| 0175h | | | | | |
| 0176h | | | | | |
| 0177h | | | | | |
| 0178h | | | | | |
| 0179h | | | | | |
| 017Ah | | | | | |
| 017Bh | | | | | |
| 017Ch | | | | | |
| 017Dh | | | | | |
| 017Eh | | | | | |
| 017Fh | | | | | |

X: Undefined

NOTE:

- Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information (7) ⁽²⁾

| Address | Register | Symbol | After Reset |
|---------|--|--------|-------------|
| 0180h | | | |
| 0181h | | | |
| 0182h | | | |
| 0183h | | | |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | | | |
| 0189h | | | |
| 018Ah | | | |
| 018Bh | | | |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | | | |
| 018Fh | | | |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | | | |
| 01B3h | | | |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 ⁽¹⁾ | FMR1 | 0X00XX0Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 ⁽¹⁾ | FMR0 | 00000001b |
| 01B8h | | | 00h |
| 01B9h | Address Match Interrupt Register 2 | RMAD2 | 00h |
| 01BAh | | | X0h |
| 01BBh | Address Match Interrupt Enable Register 2 | AIER2 | XXXXXX00b |
| 01BCh | | | 00h |
| 01BDh | Address Match Interrupt Register 3 | RMAD3 | 00h |
| 01BEh | | | X0h |
| 01BFh | | | |

X: Undefined

NOTES:

1. These registers are included in the flash memory version. Cannot be accessed by users in the mask ROM version.
2. Blank spaces are reserved. No access is allowed.

Table 4.8 SFR Information (8) ⁽¹⁾

| Address | Register | Symbol | After Reset |
|---------|---|--------|-------------|
| 01C0h | Timer B3, B4, B5 Count Start Flag | TBSR | 000XXXXXb |
| 01C1h | | | |
| 01C2h | | | XXh |
| 01C3h | Timer A1-1 Register | TA11 | XXh |
| 01C4h | | | XXh |
| 01C5h | Timer A2-1 Register | TA21 | XXh |
| 01C6h | | | XXh |
| 01C7h | Timer A4-1 Register | TA41 | XXh |
| 01C8h | Three-Phase PWM Control Register 0 | INVC0 | 00h |
| 01C9h | Three-Phase PWM Control Register 1 | INVC1 | 00h |
| 01CAh | Three-Phase Output Buffer Register 0 | IDB0 | 00111111b |
| 01CBh | Three-Phase Output Buffer Register 1 | IDB1 | 00111111b |
| 01CCh | Dead Time Timer | DTT | XXh |
| 01CDh | Timer B2 Interrupt Generation Frequency Set Counter | ICTB2 | XXh |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | XXh |
| 01D1h | Timer B3 Register | TB3 | XXh |
| 01D2h | | | XXh |
| 01D3h | Timer B4 Register | TB4 | XXh |
| 01D4h | | | XXh |
| 01D5h | Timer B5 Register | TB5 | XXh |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | Timer B3 Mode Register | TB3MR | 00XX0000b |
| 01DCh | Timer B4 Mode Register | TB4MR | 00XX0000b |
| 01DDh | Timer B5 Mode Register | TB5MR | 00XX0000b |
| 01DEh | Interrupt Source Select Register 0 | IFSR0 | 00XX0000b |
| 01DFh | Interrupt Source Select Register 1 | IFSR1 | 00h |
| 01E0h | SI/O3 Transmit/Receive Register | S3TRR | XXh |
| 01E1h | | | |
| 01E2h | SI/O3 Control Register | S3C | 01000000b |
| 01E3h | SI/O3 Bit Rate Register | S3BRG | XXh |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 01EDh | UART0 Special Mode Register 3 | U0SMR3 | 000X0X0Xb |
| 01EEh | UART0 Special Mode Register 2 | U0SMR2 | X0000000b |
| 01EFh | UART0 Special Mode Register | U0SMR | X0000000b |
| 01F0h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 01F1h | UART1 Special Mode Register 3 | U1SMR3 | 000X0X0Xb |
| 01F2h | UART1 Special Mode Register 2 | U1SMR2 | X0000000b |
| 01F3h | UART1 Special Mode Register | U1SMR | X0000000b |
| 01F4h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 01F5h | UART2 Special Mode Register 3 | U2SMR3 | 000X0X0Xb |
| 01F6h | UART2 Special Mode Register 2 | U2SMR2 | X0000000b |
| 01F7h | UART2 Special Mode Register | U2SMR | X0000000b |
| 01F8h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 01F9h | UART2 Bit Rate Register | U2BRG | XXh |
| 01FAh | | | XXh |
| 01FBh | UART2 Transmit Buffer Register | U2TB | XXh |
| 01FCh | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 01FDh | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 01FEh | | | XXh |
| 01FFh | UART2 Receive Buffer Register | U2RB | XXh |

X: Undefined

NOTE:

- Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information (9)

| Address | Register | Symbol | After Reset |
|---------|------------------------------------|----------|-------------|
| 0200h | CAN0 Message Control Register 0 | COMCTL0 | 00h |
| 0201h | CAN0 Message Control Register 1 | COMCTL1 | 00h |
| 0202h | CAN0 Message Control Register 2 | COMCTL2 | 00h |
| 0203h | CAN0 Message Control Register 3 | COMCTL3 | 00h |
| 0204h | CAN0 Message Control Register 4 | COMCTL4 | 00h |
| 0205h | CAN0 Message Control Register 5 | COMCTL5 | 00h |
| 0206h | CAN0 Message Control Register 6 | COMCTL6 | 00h |
| 0207h | CAN0 Message Control Register 7 | COMCTL7 | 00h |
| 0208h | CAN0 Message Control Register 8 | COMCTL8 | 00h |
| 0209h | CAN0 Message Control Register 9 | COMCTL9 | 00h |
| 020Ah | CAN0 Message Control Register 10 | COMCTL10 | 00h |
| 020Bh | CAN0 Message Control Register 11 | COMCTL11 | 00h |
| 020Ch | CAN0 Message Control Register 12 | COMCTL12 | 00h |
| 020Dh | CAN0 Message Control Register 13 | COMCTL13 | 00h |
| 020Eh | CAN0 Message Control Register 14 | COMCTL14 | 00h |
| 020Fh | CAN0 Message Control Register 15 | COMCTL15 | 00h |
| 0210h | CAN0 Control Register | C0CTLR | X0000001b |
| 0211h | | | XX0X0000b |
| 0212h | CAN0 Status Register | C0STR | 00h |
| 0213h | | | X0000001b |
| 0214h | CAN0 Slot Status Register | C0SSTR | 00h |
| 0215h | | | 00h |
| 0216h | CAN0 Interrupt Control Register | C0ICR | 00h |
| 0217h | | | 00h |
| 0218h | CAN0 Extended ID Register | C0IDR | 00h |
| 0219h | | | 00h |
| 021Ah | CAN0 Configuration Register | C0CONR | XXh |
| 021Bh | | | XXh |
| 021Ch | CAN0 Receive Error Count Register | C0RECR | 00h |
| 021Dh | CAN0 Transmit Error Count Register | C0TECR | 00h |
| 021Eh | CAN0 Time Stamp Register | C0TSR | 00h |
| 021Fh | | | 00h |
| 0220h | CAN1 Message Control Register 0 | C1MCTL0 | 00h |
| 0221h | CAN1 Message Control Register 1 | C1MCTL1 | 00h |
| 0222h | CAN1 Message Control Register 2 | C1MCTL2 | 00h |
| 0223h | CAN1 Message Control Register 3 | C1MCTL3 | 00h |
| 0224h | CAN1 Message Control Register 4 | C1MCTL4 | 00h |
| 0225h | CAN1 Message Control Register 5 | C1MCTL5 | 00h |
| 0226h | CAN1 Message Control Register 6 | C1MCTL6 | 00h |
| 0227h | CAN1 Message Control Register 7 | C1MCTL7 | 00h |
| 0228h | CAN1 Message Control Register 8 | C1MCTL8 | 00h |
| 0229h | CAN1 Message Control Register 9 | C1MCTL9 | 00h |
| 022Ah | CAN1 Message Control Register 10 | C1MCTL10 | 00h |
| 022Bh | CAN1 Message Control Register 11 | C1MCTL11 | 00h |
| 022Ch | CAN1 Message Control Register 12 | C1MCTL12 | 00h |
| 022Dh | CAN1 Message Control Register 13 | C1MCTL13 | 00h |
| 022Eh | CAN1 Message Control Register 14 | C1MCTL14 | 00h |
| 022Fh | CAN1 Message Control Register 15 | C1MCTL15 | 00h |
| 0230h | CAN1 Control Register | C1CTLR | X0000001b |
| 0231h | | | XX0X0000b |
| 0232h | CAN1 Status Register | C1STR | 00h |
| 0233h | | | X0000001b |
| 0234h | CAN1 Slot Status Register | C1SSTR | 00h |
| 0235h | | | 00h |
| 0236h | CAN1 Interrupt Control Register | C1ICR | 00h |
| 0237h | | | 00h |
| 0238h | CAN1 Extended ID Register | C1IDR | 00h |
| 0239h | | | 00h |
| 023Ah | CAN1 Configuration Register | C1CONR | XXh |
| 023Bh | | | XXh |
| 023Ch | CAN1 Receive Error Count Register | C1RECR | 00h |
| 023Dh | CAN1 Transmit Error Count Register | C1TECR | 00h |
| 023Eh | CAN1 Time Stamp Register | C1TSR | 00h |
| 023Fh | | | 00h |

X: Undefined

Table 4.10 SFR Information (10) ⁽¹⁾

| Address | Register | Symbol | After Reset |
|---------|---|--------|-------------|
| 0240h | | | |
| 0241h | | | |
| 0242h | | | |
| 0243h | CAN0 Acceptance Filter Support Register | C0AFS | XXh |
| 0244h | | | XXh |
| 0245h | CAN1 Acceptance Filter Support Register | C1AFS | XXh |
| 0246h | | | |
| 0247h | | | |
| 0248h | | | |
| 0249h | | | |
| 024Ah | | | |
| 024Bh | | | |
| 024Ch | | | |
| 024Dh | | | |
| 024Eh | | | |
| 024Fh | | | |
| 0250h | | | |
| 0251h | | | |
| 0252h | | | |
| 0253h | | | |
| 0254h | | | |
| 0255h | | | |
| 0256h | | | |
| 0257h | | | |
| 0258h | | | |
| 0259h | | | |
| 025Ah | | | |
| 025Bh | | | |
| 025Ch | | | |
| 025Dh | | | |
| 025Eh | Peripheral Clock Select Register | PCLKR | 00h |
| 025Fh | CAN0/1 Clock Select Register | CCLKR | 00h |
| 0260h | | | XXh |
| 0261h | | | XXh |
| 0262h | CAN1 Message Box 0: Identifier / DLC | | XXh |
| 0263h | | | XXh |
| 0264h | | | XXh |
| 0265h | | | XXh |
| 0266h | | | XXh |
| 0267h | | | XXh |
| 0268h | | | XXh |
| 0269h | CAN1 Message Box 0: Data Field | | XXh |
| 026Ah | | | XXh |
| 026Bh | | | XXh |
| 026Ch | | | XXh |
| 026Dh | | | XXh |
| 026Eh | CAN1 Message Box 0:Time Stamp | | XXh |
| 026Fh | | | XXh |
| 0270h | | | XXh |
| 0271h | | | XXh |
| 0272h | CAN1 Message Box 1: Identifier / DLC | | XXh |
| 0273h | | | XXh |
| 0274h | | | XXh |
| 0275h | | | XXh |
| 0276h | | | XXh |
| 0277h | | | XXh |
| 0278h | | | XXh |
| 0279h | CAN1 Message Box 1: Data Field | | XXh |
| 027Ah | | | XXh |
| 027Bh | | | XXh |
| 027Ch | | | XXh |
| 027Dh | | | XXh |
| 027Eh | CAN1 Message Box 1:Time Stamp | | XXh |
| 027Fh | | | XXh |

X: Undefined

NOTE:

- Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11)

| Address | Register | Symbol | After Reset | | |
|---------|--------------------------------------|--------|--------------------------------------|--|-----|
| 0280h | CAN1 Message Box 2: Identifier / DLC | | XXh | | |
| 0281h | | | XXh | | |
| 0282h | | | XXh | | |
| 0283h | | | XXh | | |
| 0284h | | | XXh | | |
| 0285h | | | XXh | | |
| 0286h | CAN1 Message Box 2: Data Field | | XXh | | |
| 0287h | | | XXh | | |
| 0288h | | | XXh | | |
| 0289h | | | XXh | | |
| 028Ah | | | XXh | | |
| 028Bh | | | XXh | | |
| 028Ch | CAN1 Message Box 2: Time Stamp | | XXh | | |
| 028Dh | | | XXh | | |
| 028Eh | | | XXh | | |
| 028Fh | | | XXh | | |
| 0290h | | | CAN1 Message Box 3: Identifier / DLC | | XXh |
| 0291h | | | | | XXh |
| 0292h | XXh | | | | |
| 0293h | XXh | | | | |
| 0294h | XXh | | | | |
| 0295h | XXh | | | | |
| 0296h | CAN1 Message Box 3: Data Field | | XXh | | |
| 0297h | | | XXh | | |
| 0298h | | | XXh | | |
| 0299h | | | XXh | | |
| 029Ah | | | XXh | | |
| 029Bh | | | XXh | | |
| 029Ch | CAN1 Message Box 3: Time Stamp | | XXh | | |
| 029Dh | | | XXh | | |
| 029Eh | | | XXh | | |
| 029Fh | | | XXh | | |
| 02A0h | | | CAN1 Message Box 4: Identifier / DLC | | XXh |
| 02A1h | | | | | XXh |
| 02A2h | XXh | | | | |
| 02A3h | XXh | | | | |
| 02A4h | XXh | | | | |
| 02A5h | XXh | | | | |
| 02A6h | CAN1 Message Box 4: Data Field | | XXh | | |
| 02A7h | | | XXh | | |
| 02A8h | | | XXh | | |
| 02A9h | | | XXh | | |
| 02AAh | | | XXh | | |
| 02ABh | | | XXh | | |
| 02ACh | CAN1 Message Box 4: Time Stamp | | XXh | | |
| 02ADh | | | XXh | | |
| 02AEh | | | XXh | | |
| 02AFh | | | XXh | | |
| 02B0h | | | CAN1 Message Box 5: Identifier / DLC | | XXh |
| 02B1h | | | | | XXh |
| 02B2h | XXh | | | | |
| 02B3h | XXh | | | | |
| 02B4h | XXh | | | | |
| 02B5h | XXh | | | | |
| 02B6h | CAN1 Message Box 5: Data Field | | XXh | | |
| 02B7h | | | XXh | | |
| 02B8h | | | XXh | | |
| 02B9h | | | XXh | | |
| 02BAh | | | XXh | | |
| 02BBh | | | XXh | | |
| 02BCh | CAN1 Message Box 5: Time Stamp | | XXh | | |
| 02BDh | | | XXh | | |
| 02BEh | | | XXh | | |
| 02BFh | | | XXh | | |

X: Undefined

Table 4.12 SFR Information (12)

| Address | Register | Symbol | After Reset | | |
|---------|--------------------------------------|--------|--------------------------------------|--|-----|
| 02C0h | CAN1 Message Box 6: Identifier / DLC | | XXh | | |
| 02C1h | | | XXh | | |
| 02C2h | | | XXh | | |
| 02C3h | | | XXh | | |
| 02C4h | | | XXh | | |
| 02C5h | | | XXh | | |
| 02C6h | CAN1 Message Box 6: Data Field | | XXh | | |
| 02C7h | | | XXh | | |
| 02C8h | | | XXh | | |
| 02C9h | | | XXh | | |
| 02CAh | | | XXh | | |
| 02CBh | | | XXh | | |
| 02CCh | CAN1 Message Box 6: Time Stamp | | XXh | | |
| 02CDh | | | XXh | | |
| 02CEh | | | XXh | | |
| 02CFh | | | XXh | | |
| 02D0h | | | CAN1 Message Box 7: Identifier / DLC | | XXh |
| 02D1h | | | | | XXh |
| 02D2h | XXh | | | | |
| 02D3h | XXh | | | | |
| 02D4h | XXh | | | | |
| 02D5h | XXh | | | | |
| 02D6h | CAN1 Message Box 7: Data Field | | XXh | | |
| 02D7h | | | XXh | | |
| 02D8h | | | XXh | | |
| 02D9h | | | XXh | | |
| 02DAh | | | XXh | | |
| 02DBh | | | XXh | | |
| 02DCh | CAN1 Message Box 7: Time Stamp | | XXh | | |
| 02DDh | | | XXh | | |
| 02DEh | | | XXh | | |
| 02DFh | | | XXh | | |
| 02E0h | | | CAN1 Message Box 8: Identifier / DLC | | XXh |
| 02E1h | | | | | XXh |
| 02E2h | XXh | | | | |
| 02E3h | XXh | | | | |
| 02E4h | XXh | | | | |
| 02E5h | XXh | | | | |
| 02E6h | CAN1 Message Box 8: Data Field | | XXh | | |
| 02E7h | | | XXh | | |
| 02E8h | | | XXh | | |
| 02E9h | | | XXh | | |
| 02EAh | | | XXh | | |
| 02EBh | | | XXh | | |
| 02ECh | CAN1 Message Box 8: Time Stamp | | XXh | | |
| 02EDh | | | XXh | | |
| 02EEh | | | XXh | | |
| 02EFh | | | XXh | | |
| 02F0h | | | CAN1 Message Box 9: Identifier / DLC | | XXh |
| 02F1h | | | | | XXh |
| 02F2h | XXh | | | | |
| 02F3h | XXh | | | | |
| 02F4h | XXh | | | | |
| 02F5h | XXh | | | | |
| 02F6h | CAN1 Message Box 9: Data Field | | XXh | | |
| 02F7h | | | XXh | | |
| 02F8h | | | XXh | | |
| 02F9h | | | XXh | | |
| 02FAh | | | XXh | | |
| 02FBh | | | XXh | | |
| 02FCh | CAN1 Message Box 9: Time Stamp | | XXh | | |
| 02FDh | | | XXh | | |
| 02FEh | | | XXh | | |
| 02FFh | | | XXh | | |

X: Undefined

Table 4.13 SFR Information (13)

| Address | Register | Symbol | After Reset | | |
|---------|---------------------------------------|--------|---------------------------------------|--|-----|
| 0300h | CAN1 Message Box 10: Identifier / DLC | | XXh | | |
| 0301h | | | XXh | | |
| 0302h | | | XXh | | |
| 0303h | | | XXh | | |
| 0304h | | | XXh | | |
| 0305h | | | XXh | | |
| 0306h | CAN1 Message Box 10: Data Field | | XXh | | |
| 0307h | | | XXh | | |
| 0308h | | | XXh | | |
| 0309h | | | XXh | | |
| 030Ah | | | XXh | | |
| 030Bh | | | XXh | | |
| 030Ch | CAN1 Message Box 10: Time Stamp | | XXh | | |
| 030Dh | | | XXh | | |
| 030Eh | | | XXh | | |
| 030Fh | | | XXh | | |
| 0310h | | | CAN1 Message Box 11: Identifier / DLC | | XXh |
| 0311h | | | | | XXh |
| 0312h | XXh | | | | |
| 0313h | XXh | | | | |
| 0314h | XXh | | | | |
| 0315h | XXh | | | | |
| 0316h | CAN1 Message Box 11: Data Field | | XXh | | |
| 0317h | | | XXh | | |
| 0318h | | | XXh | | |
| 0319h | | | XXh | | |
| 031Ah | | | XXh | | |
| 031Bh | | | XXh | | |
| 031Ch | CAN1 Message Box 11: Time Stamp | | XXh | | |
| 031Dh | | | XXh | | |
| 031Eh | | | XXh | | |
| 031Fh | | | XXh | | |
| 0320h | | | CAN1 Message Box 12: Identifier / DLC | | XXh |
| 0321h | | | | | XXh |
| 0322h | XXh | | | | |
| 0323h | XXh | | | | |
| 0324h | XXh | | | | |
| 0325h | XXh | | | | |
| 0326h | CAN1 Message Box 12: Data Field | | XXh | | |
| 0327h | | | XXh | | |
| 0328h | | | XXh | | |
| 0329h | | | XXh | | |
| 032Ah | | | XXh | | |
| 032Bh | | | XXh | | |
| 032Ch | CAN1 Message Box 12: Time Stamp | | XXh | | |
| 032Dh | | | XXh | | |
| 032Eh | | | XXh | | |
| 032Fh | | | XXh | | |
| 0330h | | | CAN1 Message Box 13: Identifier / DLC | | XXh |
| 0331h | | | | | XXh |
| 0332h | XXh | | | | |
| 0333h | XXh | | | | |
| 0334h | XXh | | | | |
| 0335h | XXh | | | | |
| 0336h | CAN1 Message Box 13: Data Field | | XXh | | |
| 0337h | | | XXh | | |
| 0338h | | | XXh | | |
| 0339h | | | XXh | | |
| 033Ah | | | XXh | | |
| 033Bh | | | XXh | | |
| 033Ch | CAN1 Message Box 13: Time Stamp | | XXh | | |
| 033Dh | | | XXh | | |
| 033Eh | | | XXh | | |
| 033Fh | | | XXh | | |

X: Undefined

Table 4.14 SFR Information (14) ⁽¹⁾

| Address | Register | Symbol | After Reset | | |
|---------|---------------------------------------|--------|---------------------------------------|-------|-----|
| 0340h | CAN1 Message Box 14: Identifier / DLC | | XXh | | |
| 0341h | | | XXh | | |
| 0342h | | | XXh | | |
| 0343h | | | XXh | | |
| 0344h | | | XXh | | |
| 0345h | | | XXh | | |
| 0346h | CAN1 Message Box 14: Data Field | | XXh | | |
| 0347h | | | XXh | | |
| 0348h | | | XXh | | |
| 0349h | | | XXh | | |
| 034Ah | | | XXh | | |
| 034Bh | | | XXh | | |
| 034Ch | CAN1 Message Box 14: Time Stamp | | XXh | | |
| 034Dh | | | XXh | | |
| 034Eh | | | XXh | | |
| 034Fh | | | XXh | | |
| 0350h | | | CAN1 Message Box 15: Identifier / DLC | | XXh |
| 0351h | | | | | XXh |
| 0352h | XXh | | | | |
| 0353h | XXh | | | | |
| 0354h | XXh | | | | |
| 0355h | XXh | | | | |
| 0356h | CAN1 Message Box 15: Data Field | | XXh | | |
| 0357h | | | XXh | | |
| 0358h | | | XXh | | |
| 0359h | | | XXh | | |
| 035Ah | | | XXh | | |
| 035Bh | | | XXh | | |
| 035Ch | CAN1 Message Box 15: Time Stamp | | XXh | | |
| 035Dh | | | XXh | | |
| 035Eh | | | XXh | | |
| 035Fh | | | XXh | | |
| 0360h | | | CAN1 Global Mask Register | C1GMR | XXh |
| 0361h | | | | | XXh |
| 0362h | XXh | | | | |
| 0363h | XXh | | | | |
| 0364h | XXh | | | | |
| 0365h | XXh | | | | |
| 0366h | CAN1 Local Mask A Register | C1LMAR | XXh | | |
| 0367h | | | XXh | | |
| 0368h | | | XXh | | |
| 0369h | | | XXh | | |
| 036Ah | | | XXh | | |
| 036Bh | | | XXh | | |
| 036Ch | CAN1 Local Mask B Register | C1LMBR | XXh | | |
| 036Dh | | | XXh | | |
| 036Eh | | | XXh | | |
| 036Fh | | | XXh | | |
| 0370h | | | XXh | | |
| 0371h | | | XXh | | |
| 0372h | | | | | |
| 0373h | | | | | |
| 0374h | | | | | |
| 0375h | | | | | |
| 0376h | | | | | |
| 0377h | | | | | |
| 0378h | | | | | |
| 0379h | | | | | |
| 037Ah | | | | | |
| 037Bh | | | | | |
| 037Ch | | | | | |
| 037Dh | | | | | |
| 037Eh | | | | | |
| 037Fh | | | | | |

X: Undefined

NOTE:

1. Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information (15) ⁽²⁾

| Address | Register | Symbol | After Reset |
|---------|---|--------|--------------------|
| 0380h | Count Start Flag | TABSR | 00h |
| 0381h | Clock Prescaler Reset Flag | CPSRF | 0XXXXXXb |
| 0382h | One-Shot Start Flag | ONSF | 00h |
| 0383h | Trigger Select Register | TRGSR | 00h |
| 0384h | Up/Down Flag | UDF | 00h ⁽¹⁾ |
| 0385h | | | |
| 0386h | Timer A0 Register | TA0 | XXh |
| 0387h | | | XXh |
| 0388h | Timer A1 Register | TA1 | XXh |
| 0389h | | | XXh |
| 038Ah | Timer A2 Register | TA2 | XXh |
| 038Bh | | | XXh |
| 038Ch | Timer A3 Register | TA3 | XXh |
| 038Dh | | | XXh |
| 038Eh | Timer A4 Register | TA4 | XXh |
| 038Fh | | | XXh |
| 0390h | Timer B0 Register | TB0 | XXh |
| 0391h | | | XXh |
| 0392h | Timer B1 Register | TB1 | XXh |
| 0393h | | | XXh |
| 0394h | Timer B2 Register | TB2 | XXh |
| 0395h | | | XXh |
| 0396h | Timer A0 Mode Register | TA0MR | 00h |
| 0397h | Timer A1 Mode Register | TA1MR | 00h |
| 0398h | Timer A2 Mode Register | TA2MR | 00h |
| 0399h | Timer A3 Mode Register | TA3MR | 00h |
| 039Ah | Timer A4 Mode Register | TA4MR | 00h |
| 039Bh | Timer B0 Mode Register | TB0MR | 00XX0000b |
| 039Ch | Timer B1 Mode Register | TB1MR | 00XX0000b |
| 039Dh | Timer B2 Mode Register | TB2MR | 00XX0000b |
| 039Eh | Timer B2 Special Mode Register | TB2SC | XXXXXX00b |
| 039Fh | | | |
| 03A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 03A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 03A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 03A3h | | | XXh |
| 03A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 03A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00XX0010b |
| 03A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 03A7h | | | XXh |
| 03A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 03A9h | UART1 Bit Rate Register | U1BRG | XXh |
| 03AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 03ABh | | | XXh |
| 03ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 03ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00XX0010b |
| 03AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 03AFh | | | XXh |
| 03B0h | UART Transmit/Receive Control Register 2 | UCON | X0000000b |
| 03B1h | | | |
| 03B2h | | | |
| 03B3h | | | |
| 03B4h | | | |
| 03B5h | | | |
| 03B6h | | | |
| 03B7h | | | |
| 03B8h | DMA0 Request Source Select Register | DM0SL | 00h |
| 03B9h | | | |
| 03BAh | DMA1 Request Source Select Register | DM1SL | 00h |
| 03BBh | | | |
| 03BCh | CRC Data Register | CRCD | XXh |
| 03BDh | | | XXh |
| 03BEh | CRC Input Register | CRCIN | XXh |
| 03BFh | | | |

X: Undefined

NOTES:

1. Bits TA2P to TA4P in the UDF register are set to 0 after reset. However, the contents in these bits are undefined when read.
2. Blank spaces are reserved. No access is allowed.

Table 4.16 SFR Information (16) ⁽²⁾

| Address | Register | Symbol | After Reset |
|---------|-----------------------------|--------|---------------------------------------|
| 03C0h | A/D Register 0 | AD0 | XXh |
| 03C1h | | | XXh |
| 03C2h | A/D Register 1 | AD1 | XXh |
| 03C3h | | | XXh |
| 03C4h | A/D Register 2 | AD2 | XXh |
| 03C5h | | | XXh |
| 03C6h | A/D Register 3 | AD3 | XXh |
| 03C7h | | | XXh |
| 03C8h | A/D Register 4 | AD4 | XXh |
| 03C9h | | | XXh |
| 03CAh | A/D Register 5 | AD5 | XXh |
| 03CBh | | | XXh |
| 03CCh | A/D Register 6 | AD6 | XXh |
| 03CDh | | | XXh |
| 03CEh | A/D Register 7 | AD7 | XXh |
| 03CFh | | | XXh |
| 03D0h | | | |
| 03D1h | | | |
| 03D2h | | | |
| 03D3h | | | |
| 03D4h | A/D Control Register 2 | ADCON2 | 00h |
| 03D5h | | | |
| 03D6h | A/D Control Register 0 | ADCON0 | 00000XXXb |
| 03D7h | A/D Control Register 1 | ADCON1 | 00h |
| 03D8h | D/A Register 0 | DA0 | 00h |
| 03D9h | | | |
| 03DAh | D/A Register 1 | DA1 | 00h |
| 03DBh | | | |
| 03DCh | D/A Control Register | DACON | 00h |
| 03DDh | | | |
| 03DEh | | | |
| 03DFh | | | |
| 03E0h | Port P0 Register | P0 | XXh |
| 03E1h | Port P1 Register | P1 | XXh |
| 03E2h | Port P0 Direction Register | PD0 | 00h |
| 03E3h | Port P1 Direction Register | PD1 | 00h |
| 03E4h | Port P2 Register | P2 | XXh |
| 03E5h | Port P3 Register | P3 | XXh |
| 03E6h | Port P2 Direction Register | PD2 | 00h |
| 03E7h | Port P3 Direction Register | PD3 | 00h |
| 03E8h | Port P4 Register | P4 | XXh |
| 03E9h | Port P5 Register | P5 | XXh |
| 03EAh | Port P4 Direction Register | PD4 | 00h |
| 03EBh | Port P5 Direction Register | PD5 | 00h |
| 03ECh | Port P6 Register | P6 | XXh |
| 03EDh | Port P7 Register | P7 | XXh |
| 03EEh | Port P6 Direction Register | PD6 | 00h |
| 03EFh | Port P7 Direction Register | PD7 | 00h |
| 03F0h | Port P8 Register | P8 | XXh |
| 03F1h | Port P9 Register | P9 | XXh |
| 03F2h | Port P8 Direction Register | PD8 | 00X00000b |
| 03F3h | Port P9 Direction Register | PD9 | 00h |
| 03F4h | Port P10 Register | P10 | XXh |
| 03F5h | | | |
| 03F6h | Port P10 Direction Register | PD10 | 00h |
| 03F7h | | | |
| 03F8h | | | |
| 03F9h | | | |
| 03FAh | | | |
| 03FBh | | | |
| 03FCh | Pull-up Control Register 0 | PUR0 | 00h |
| 03FDh | Pull-up Control Register 1 | PUR1 | 00000000b ⁽¹⁾ 00000010b |
| 03FEh | Pull-up Control Register 2 | PUR2 | 00h |
| 03FFh | Port Control Register | PCR | 00h |

X: Undefined

NOTES:

1. At hardware reset, the register is as follows:

- 00000000b where "L" is input to the CNVSS pin
- 00000010b where "H" is input to the CNVSS pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:

- 00000000b where bits PM01 to PM00 in the PM0 register are 00b (single-chip mode)
- 00000010b where bits PM01 to PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode)

2. Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (T/V-ver.)

Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | | Condition | Rated Value | Unit |
|------------------|-------------------------------|--|-------------------------|--|------|
| V _{CC} | Supply voltage (VCC1 = VCC2) | | VCC = AVCC | -0.3 to 6.5 | V |
| AV _{CC} | Analog supply voltage | | VCC = AVCC | -0.3 to 6.5 | V |
| V _I | Input voltage | RESET, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, VREF, XIN | | -0.3 to VCC+0.3 | V |
| | | P7_1, P9_1 | | -0.3 to 6.5 | V |
| V _O | Output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XOUT | | -0.3 to VCC+0.3 | V |
| | | P7_1, P9_1 | | -0.3 to 6.5 | V |
| P _d | Power dissipation | | T _{opr} = 25°C | 700 | mW |
| T _{opr} | Operating ambient temperature | During MCU operation | | T version: -40 to 85 V version: -40 to 125 (option) | °C |
| | | During flash memory program and erase operation | | 0 to 60 | |
| T _{stg} | Storage temperature | | | -65 to 150 | °C |

option: All options are on request basis.

Table 5.2 Recommended Operating Conditions (1) ⁽¹⁾

| Symbol | Parameter | | Standard | | | Unit |
|-----------------------|---|--|---------------------|-----------------|----------------------|------|
| | | | Min. | Typ. | Max. | |
| V _{CC} | Supply voltage (V _{CC1} = V _{CC2}) | | 4.2 | 5.0 | 5.5 | V |
| AV _{CC} | Analog supply voltage | | | V _{CC} | | V |
| V _{SS} | Supply voltage | | | 0 | | V |
| AV _{SS} | Analog supply voltage | | | 0 | | V |
| V _{IH} | HIGH input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | 0.8 V _{CC} | | V _{CC} | V |
| | | P7_1, P9_1 | 0.8 V _{CC} | | 6.5 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode) | 0.8 V _{CC} | | V _{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes) | 0.5 V _{CC} | | V _{CC} | V |
| V _{IL} | LOW input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | 0 | | 0.2 V _{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode) | 0 | | 0.2 V _{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes) | 0 | | 0.16 V _{CC} | V |
| I _{OH(peak)} | HIGH peak output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | | | -10.0 | mA |
| I _{OH(avg)} | HIGH average output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | | | -5.0 | mA |
| I _{OL(peak)} | LOW peak output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | 10.0 | mA |
| I _{OL(avg)} | LOW average output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | 5.0 | mA |

NOTES:

1. Referenced to V_{CC} = 4.2 to 5.5 V at T_{opr} = -40 to 85°C unless otherwise specified.
2. Average output current values during 100 ms period.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9, and P10 must be 80 mA max.
The total I_{OL(peak)} for ports P3, P4, P5, P6, P7, and P8_0 to P8_4 must be 80 mA max.
The total I_{OH(peak)} for ports P0, P1, and P2 must be -40 mA max.
The total I_{OH(peak)} for ports P3, P4, and P5 must be -40 mA max.
The total I_{OH(peak)} for ports P6, P7, and P8_0 to P8_4 must be -40 mA max.
The total I_{OH(peak)} for ports P8_6, P8_7, P9, and P10 must be -40 mA max.

Table 5.3 Recommended Operating Conditions (2) ⁽¹⁾

| Symbol | Parameter | | | | Standard | | | Unit |
|----------------------|---|---------|--|--------------------|----------|--------|------|------|
| | | | | | Min. | Typ. | Max. | |
| f(XIN) | Main clock input oscillation frequency ^{(2) (3) (4)} | No wait | Mask ROM version Flash memory version | VCC = 4.2 to 5.5 V | 0 | | 16 | MHz |
| f(XCIN) | Sub clock oscillation frequency | | | | | 32.768 | 50 | kHz |
| f(Ring) | On-chip oscillation frequency | | | | | 1 | | MHz |
| f(PLL) | PLL clock oscillation frequency | | | | 16 | | 20 | MHz |
| f(BCLK) | CPU operation clock | | | VCC = 4.2 to 5.5 V | 0 | | 20 | MHz |
| t _{su(PLL)} | PLL frequency synthesizer stabilization wait time | | | | | | 20 | ms |

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V at Topr = -40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency and supply voltage is shown right.
3. Execute program/erase of flash memory by VCC = 5.0 ± 0.5 V.
4. When using over 16 MHz, use PLL clock. PLL clock oscillation frequency which can be used is 16 MHz or 20 MHz.

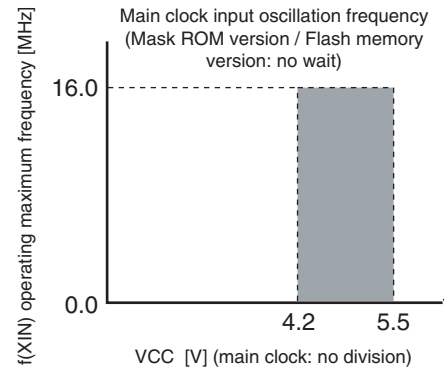


Table 5.4 Electrical Characteristics (1) ⁽¹⁾

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|----------------------------------|-----------------------|--|---------------------------|---------------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | HIGH output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | I _{OH} = -5 mA | V _{CC} -2.0 | | V _{CC} | V |
| V _{OH} | HIGH output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | I _{OH} = -200 μA | V _{CC} -0.3 | | V _{CC} | V |
| V _{OH} | HIGH output voltage | XOUT | HIGHPOWER | I _{OH} = -1 mA | 3.0 | V _{CC} | V |
| | | | LOWPOWER | I _{OH} = -0.5 mA | 3.0 | V _{CC} | |
| | HIGH output voltage | XCOUT | HIGHPOWER | With no load applied | | 2.5 | V |
| | | | LOWPOWER | With no load applied | | 1.6 | |
| V _{OL} | LOW output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | I _{OL} = 5 mA | | | 2.0 | V |
| V _{OL} | LOW output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | I _{OL} = 200 μA | | | 0.45 | V |
| V _{OL} | LOW output voltage | XOUT | HIGHPOWER | I _{OL} = 1 mA | | 2.0 | V |
| | | | LOWPOWER | I _{OL} = 0.5 mA | | 2.0 | |
| | LOW output voltage | XCOUT | HIGHPOWER | With no load applied | | 0 | V |
| | | | LOWPOWER | With no load applied | | 0 | |
| V _{T+} -V _{T-} | Hysteresis | HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, K _{I0} to K _{I3} , RXD0 to RXD2, SIN3 | | 0.2 | | 1.0 | V |
| V _{T+} -V _{T-} | Hysteresis | RESET | | 0.2 | | 2.5 | V |
| I _{IH} | HIGH input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | V _I = 5 V | | | 5.0 | μA |
| I _{IL} | LOW input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | V _I = 0 V | | | -5.0 | μA |
| R _{PULLUP} | Pull-up resistance | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | V _I = 0 V | 30 | 50 | 170 | kΩ |
| R _{IXIN} | Feedback resistance | XIN | | | 1.5 | | MΩ |
| R _{IXCIN} | Feedback resistance | XCIN | | | 15 | | MΩ |
| V _{RAM} | RAM retention voltage | | At stop mode | 2.0 | | | V |

NOTES:

1. Referenced to V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 20 MHz unless otherwise specified.

Table 5.5 Electrical Characteristics (2) ⁽¹⁾

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|-----------------|--|---|----------------------|---|--------------------------------|------|------|------|
| | | | | | Min. | Typ. | Max. | |
| I _{cc} | Power supply current (VCC = 4.2 to 5.5 V) | In single-chip mode, the output pins are open and other pins are VSS. | Mask ROM | f(BCLK) = 20 MHz, PLL operation, No division | | 18 | 32 | mA |
| | | | | On-chip oscillation, No division | | 1 | | mA |
| | | | Flash memory | f(BCLK) = 20 MHz, PLL operation, No division | | 20 | 34 | mA |
| | | | | On-chip oscillation, No division | | 1.8 | | mA |
| | | | Flash memory program | f(BCLK) = 10 MHz, VCC = 5 V | | 15 | | mA |
| | | | Flash memory erase | f(BCLK) = 10 MHz, VCC = 5 V | | 25 | | mA |
| | | | Mask ROM | f(BCLK) = 32kHz, Low power dissipation mode, ROM ⁽²⁾ | | 25 | | μA |
| | | | Flash memory | f(BCLK) = 32 kHz, Low power dissipation mode, RAM ⁽²⁾ | | 25 | | μA |
| | | | | f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory ⁽²⁾ | | 420 | | μA |
| | | | | Mask ROM Flash memory | On-chip oscillation, Wait mode | | 50 | |
| | | | Flash memory | f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity High | | 8.5 | | μA |
| | | | | f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity Low | | 3.0 | | μA |
| | | | | Stop mode, Topr = 25°C | | 0.8 | 3.0 | μA |

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at Topr = -40 to 85°C, f(BCLK) = 20 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Table 5.6 A/D Conversion Characteristics ⁽¹⁾

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---------------------|---|---------|--------------------------------|---|--|------|------------------|------|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | VREF = VCC | | | | 10 | Bit |
| INL | Integral nonlinearity error | 10 bits | VREF = VCC = 5 V | ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | | | ±3 | LSB |
| | | 8 bits | | VREF = AVCC = VCC = 5 V | External operation amp connection mode | | | ±7 |
| – | Absolute accuracy | 10 bits | VREF = VCC = 5 V | ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | | | ±3 | LSB |
| | | 8 bits | | VREF = AVCC = VCC = 5 V | External operation amp connection mode | | | ±7 |
| DNL | Differential nonlinearity error | | | | | | ±1 | LSB |
| – | Offset error | | | | | | ±3 | LSB |
| – | Gain error | | | | | | ±3 | LSB |
| R _{LADDER} | Resistor ladder | | VREF = VCC | | 10 | | 40 | kΩ |
| t _{CONV} | 10-bit conversion time, sample & hold available | | VREF = VCC = 5 V, φAD = 10 MHz | | 3.3 | | | μs |
| | 8-bit conversion time, sample & hold available | | VREF = VCC = 5 V, φAD = 10 MHz | | 2.8 | | | μs |
| t _{SAMP} | Sampling time | | | | 0.3 | | | μs |
| V _{REF} | Reference voltage | | | | 2.0 | | V _{CC} | V |
| V _{IA} | Analog input voltage | | | | 0 | | V _{REF} | V |

NOTES:

1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, –40 to 85°C unless otherwise specified.
2. φAD frequency must be 10 MHz or less.
3. When sample & hold is disabled, φAD frequency must be 250kHz or more in addition to a limit of NOTE 2.
When sample & hold is enabled, φAD frequency must be 1MHz or more in addition to a limit of NOTE 2.

Table 5.7 D/A conversion Characteristics ⁽¹⁾

| Symbol | Parameter | | Measuring condition | | Standard | | | Unit |
|-------------------|--------------------------------------|--|---------------------|--|----------|------|------|------|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | | | | | 8 | Bits |
| – | Absolute accuracy | | | | | | 1.0 | % |
| t _{su} | Setup time | | | | | | 3 | μs |
| R _o | Output resistance | | | | 4 | 10 | 20 | kΩ |
| I _{VREF} | Reference power supply input current | | (NOTE 2) | | | | 1.5 | mA |

NOTES:

1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to 00h.
The resistor ladder of the A/D converter is not included. Also, the I_{VREF} will flow even if VREF is disconnected by the ADCON1 register.

Table 5.8 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|--------------|---|---------------------|----------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during powering-on | VCC = 4.2 to 5.5 V | | | 2 | ms |
| $t_{d(R-S)}$ | STOP release time | | | | 150 | μ s |
| $t_{d(W-S)}$ | Low power dissipation mode wait mode release time | | | | 150 | μ s |

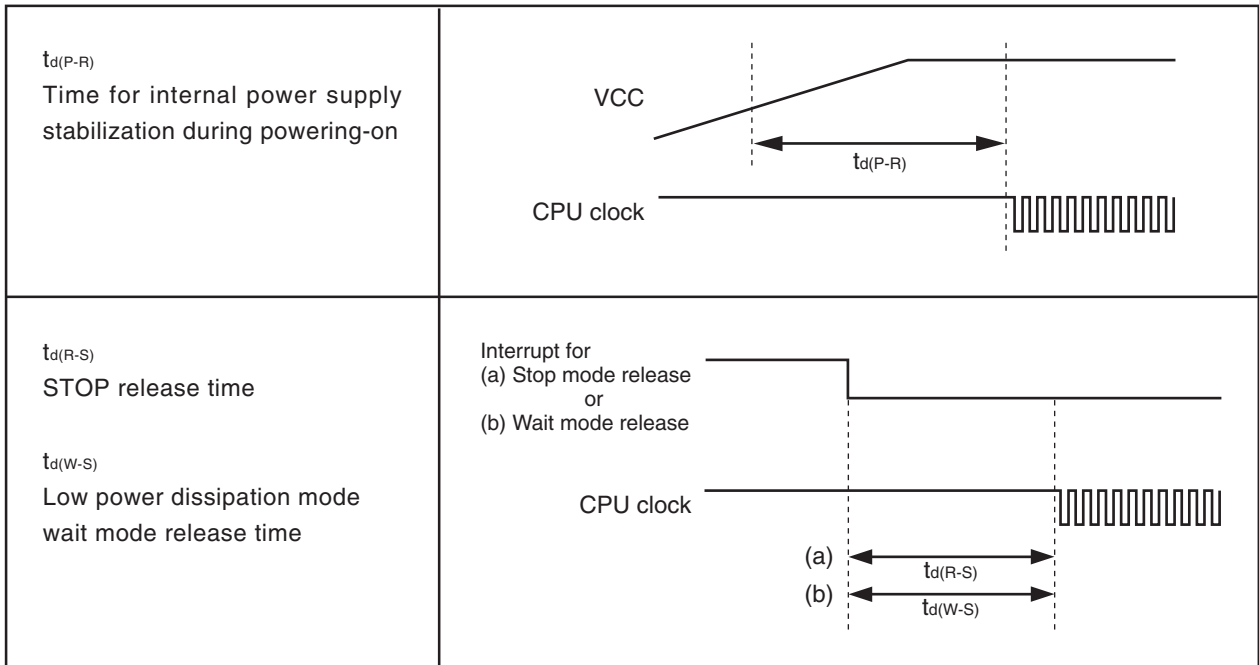


Figure 5.1 Power Supply Circuit Timing Diagram

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)****Table 5.9 External Clock Input (XIN Input)**

| Symbol | Parameter | Standard | | Unit |
|-------------------|---------------------------------------|----------|------|------|
| | | Min. | Max. | |
| t _c | External clock input cycle time | 62.5 | | ns |
| t _{w(H)} | External clock input HIGH pulse width | 25 | | ns |
| t _{w(L)} | External clock input LOW pulse width | 25 | | ns |
| t _r | External clock rise time | | 15 | ns |
| t _f | External clock fall time | | 15 | ns |

Table 5.10 Memory Expansion Mode and Microprocessor Mode

| Symbol | Parameter | Standard | | Unit |
|----------------------------|--|----------|----------|------|
| | | Min. | Max. | |
| t _{ac1(RD-DB)} | Data input access time (for setting with no wait) | | (NOTE 1) | ns |
| t _{ac2(RD-DB)} | Data input access time (for setting with wait) | | (NOTE 2) | ns |
| t _{ac3(RD-DB)} | Data input access time (when accessing multiplexed bus area) | | (NOTE 3) | ns |
| t _{su(DB-RD)} | Data input setup time | 40 | | ns |
| t _{su(RDY-BCLK)} | RDY input setup time | 30 | | ns |
| t _{su(HOLD-BCLK)} | HOLD input setup time | 40 | | ns |
| t _{h(RD-DB)} | Data input hold time | 0 | | ns |
| t _{h(BCLK-RDY)} | RDY input hold time | 0 | | ns |
| t _{h(BCLK-HOLD)} | HOLD input hold time | 0 | | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.11 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 40 | | ns |

Table 5.12 Timer A Input (Gating Input in Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 200 | | ns |

Table 5.13 Timer A Input (External Trigger Input in One-shot Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 100 | | ns |

Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 100 | | ns |

Table 5.15 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|------------------|-------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT input cycle time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT input HIGH pulse width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT input LOW pulse width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT input setup time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT input hold time | 400 | | ns |

Table 5.16 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|----------------------|-------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT input setup time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN input setup time | 200 | | ns |

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.17 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|--------------|--|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on both edges) | 80 | | ns |

Table 5.18 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width | 200 | | ns |

Table 5.19 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width | 200 | | ns |

Table 5.20 A/D Trigger Input

| Symbol | Parameter | Standard | | Unit |
|--------------|--|----------|------|------|
| | | Min. | Max. | |
| $t_{c(AD)}$ | ADTRG $\bar{}$ input cycle time (trigger able minimum) | 1000 | | ns |
| $t_{w(ADL)}$ | ADTRG $\bar{}$ input LOW pulse width | 125 | | ns |

Table 5.21 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input HIGH pulse width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi input LOW pulse width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | | ns |

Table 5.22 External Interrupt INTi Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | INTi input HIGH pulse width | 250 | | ns |
| $t_{w(INL)}$ | INTi input LOW pulse width | 250 | | ns |

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|--|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.2 | | 25 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | 0 | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 25 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (BCLK-ALE) | ALE signal output delay time | | | 15 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time | | -4 | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 25 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 25 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) ⁽³⁾ | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) ⁽³⁾ | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | 40 | ns | |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad f(\text{BCLK}) \text{ is } 12.5 \text{ MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF, R = 1 kΩ, hold time of output "L" level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$

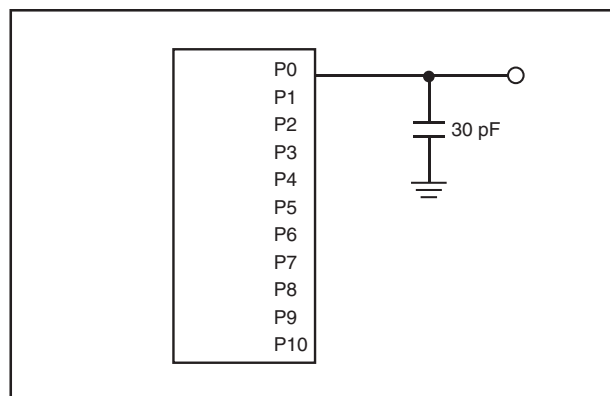
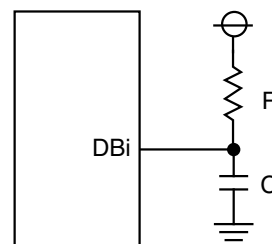


Figure 5.2 Port P0 to P10 Measurement Circuit

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|--|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.2 | | 25 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | 0 | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 25 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (BCLK-ALE) | ALE signal output delay time | | | 15 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time | | -4 | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 25 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 25 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) ⁽³⁾ | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) ⁽³⁾ | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | 40 | ns | |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

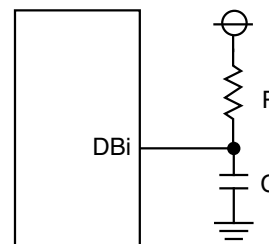
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF,

R = 1 kΩ, hold time of output "L" level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$



Switching Characteristics**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.25 Memory Expansion Mode and Microprocessor Mode
(for 2- to 3-wait setting, external area access and multiplexed bus selection)**

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|---|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.2 | | 25 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | (NOTE 1) | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 25 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-CS) | Chip select output hold time (in relation to RD) | | (NOTE 1) | | ns |
| t _h (WR-CS) | Chip select output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 25 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 25 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | | 40 | ns |
| t _d (BCLK-ALE) | ALE signal output delay time (in relation to BCLK) | | | 15 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time (in relation to BCLK) | | –4 | | ns |
| t _d (AD-ALE) | ALE signal output delay time (in relation to Address) | | (NOTE 3) | | ns |
| t _h (ALE-AD) | ALE signal output hold time (in relation to Address) | | (NOTE 4) | | ns |
| t _d (AD-RD) | RD signal output delay from the end of Address | | 0 | | ns |
| t _d (AD-WR) | WR signal output delay from the end of Address | | 0 | | ns |
| t _{dZ} (RD-AD) | Address output floating start time | | | 8 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 \text{ [ns]}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \text{ [ns]}$$

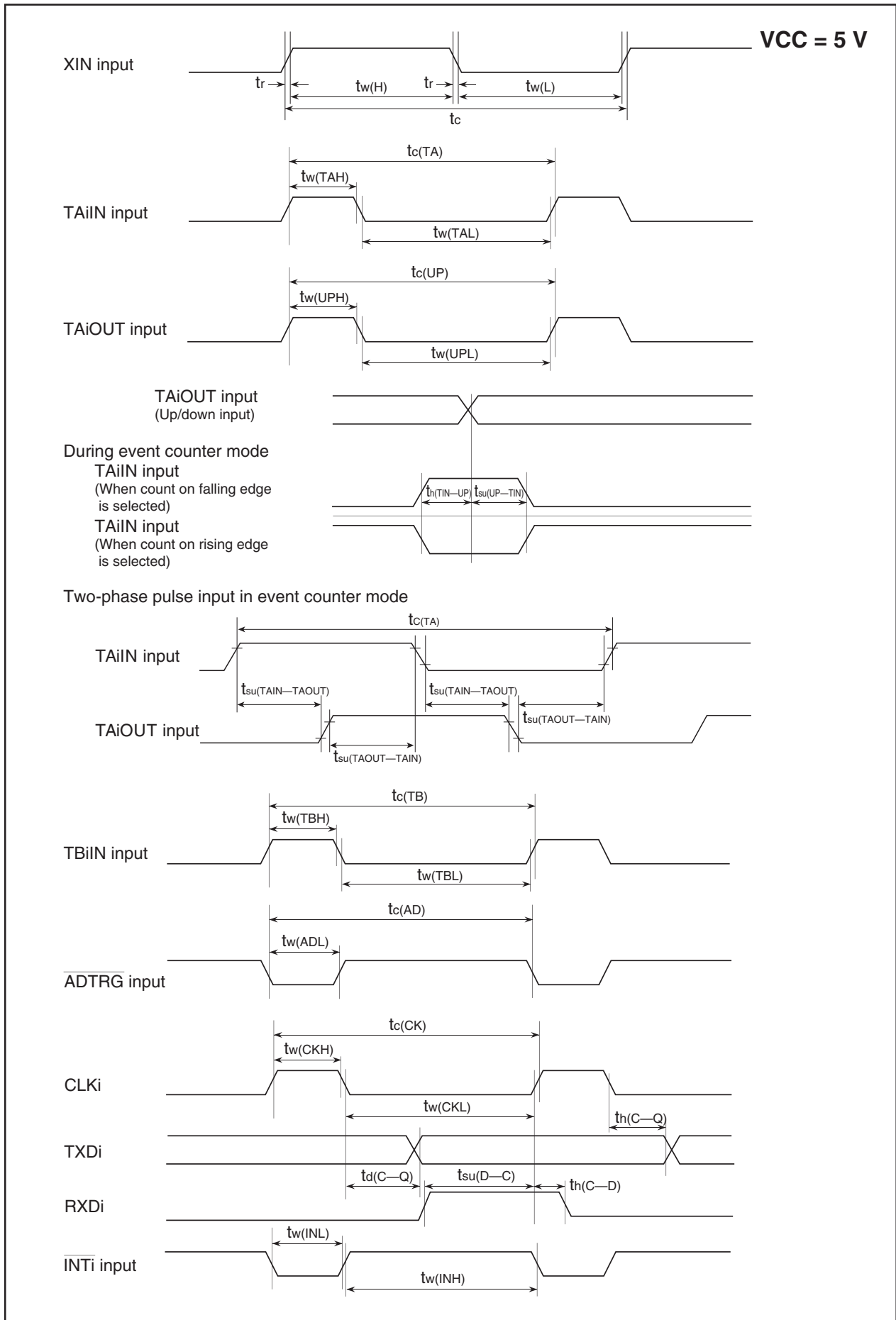


Figure 5.3 Timing Diagram (1)

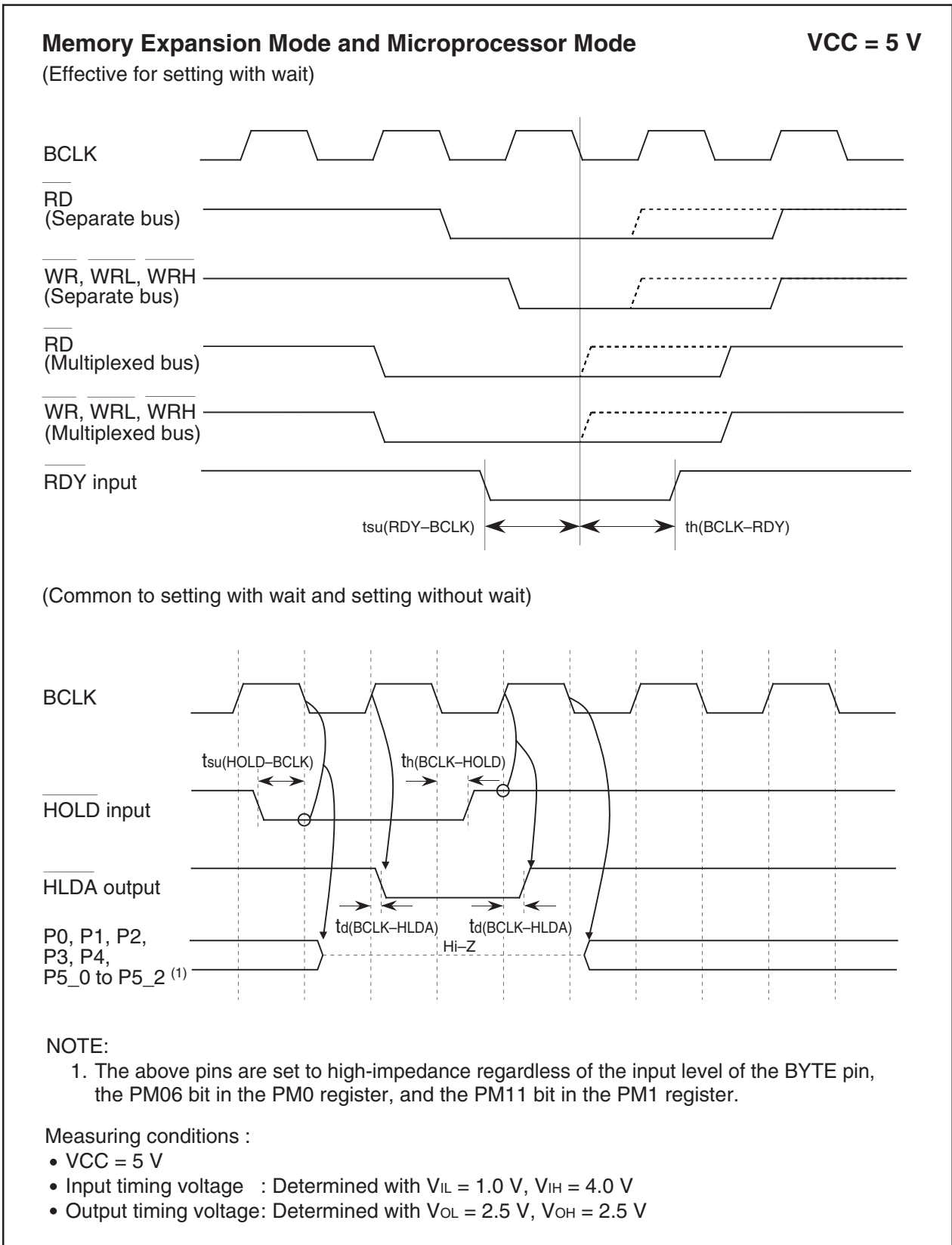


Figure 5.4 Timing Diagram (2)

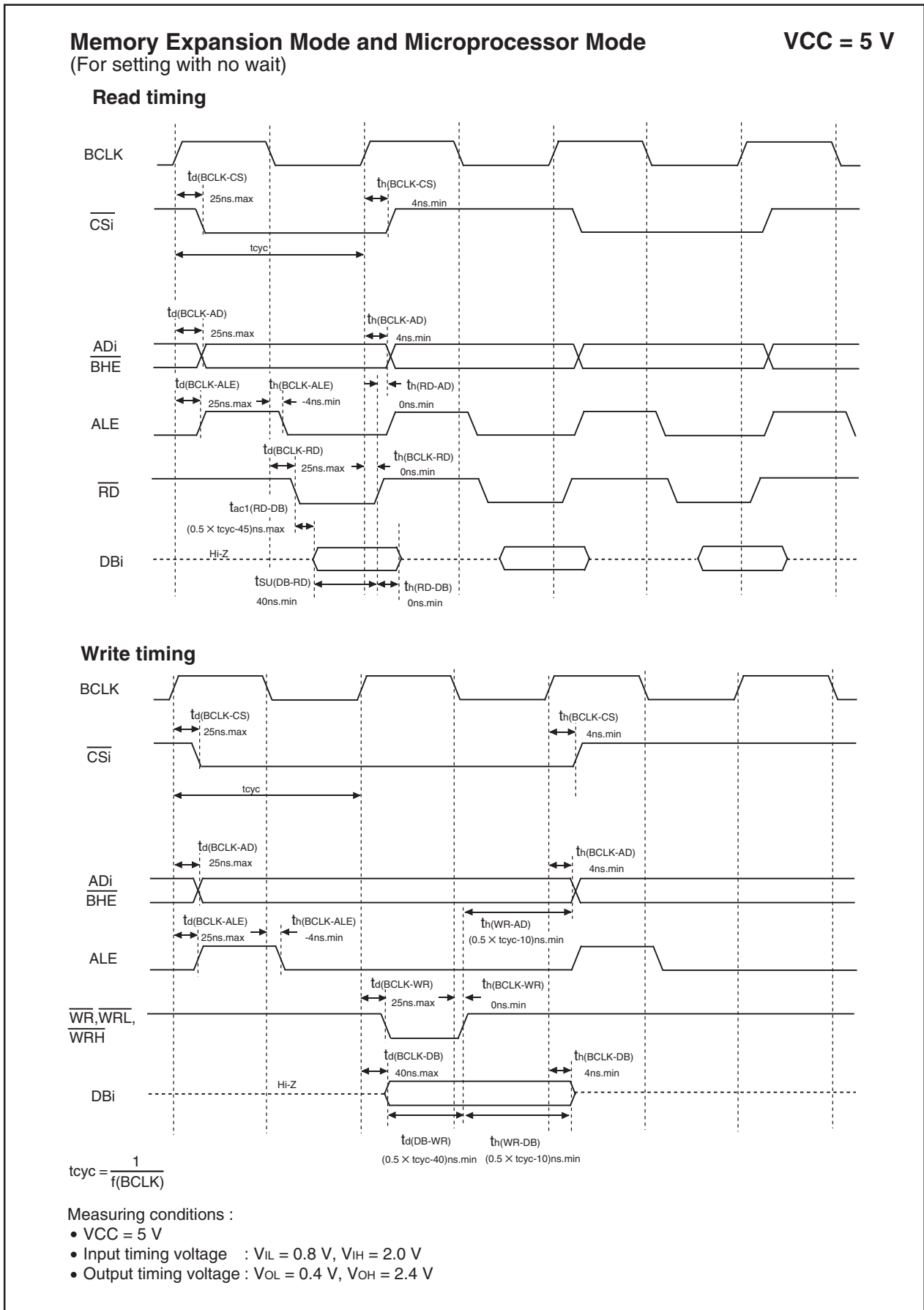


Figure 5.5 Timing Diagram (3)

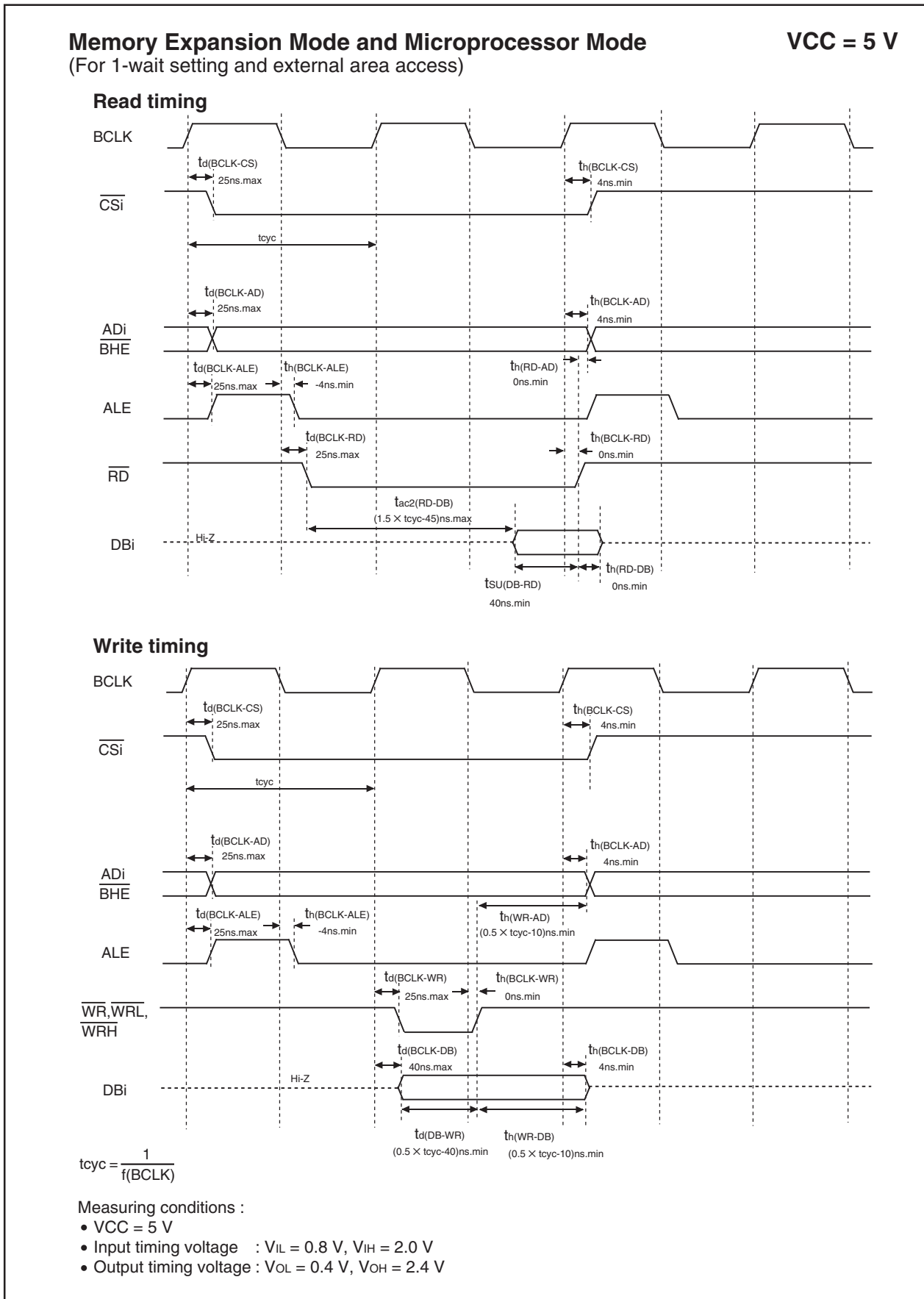


Figure 5.6 Timing Diagram (4)

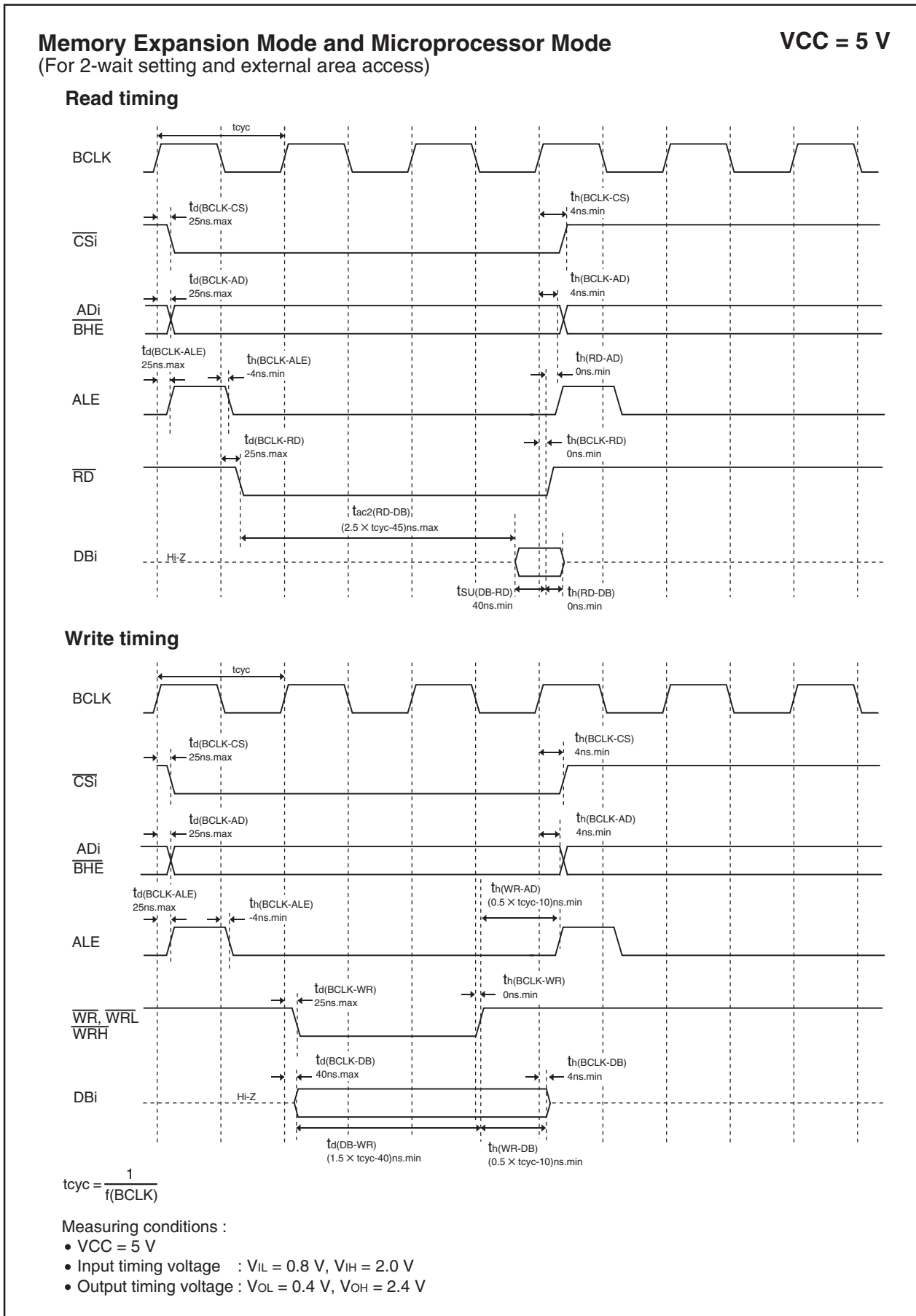


Figure 5.7 Timing Diagram (5)

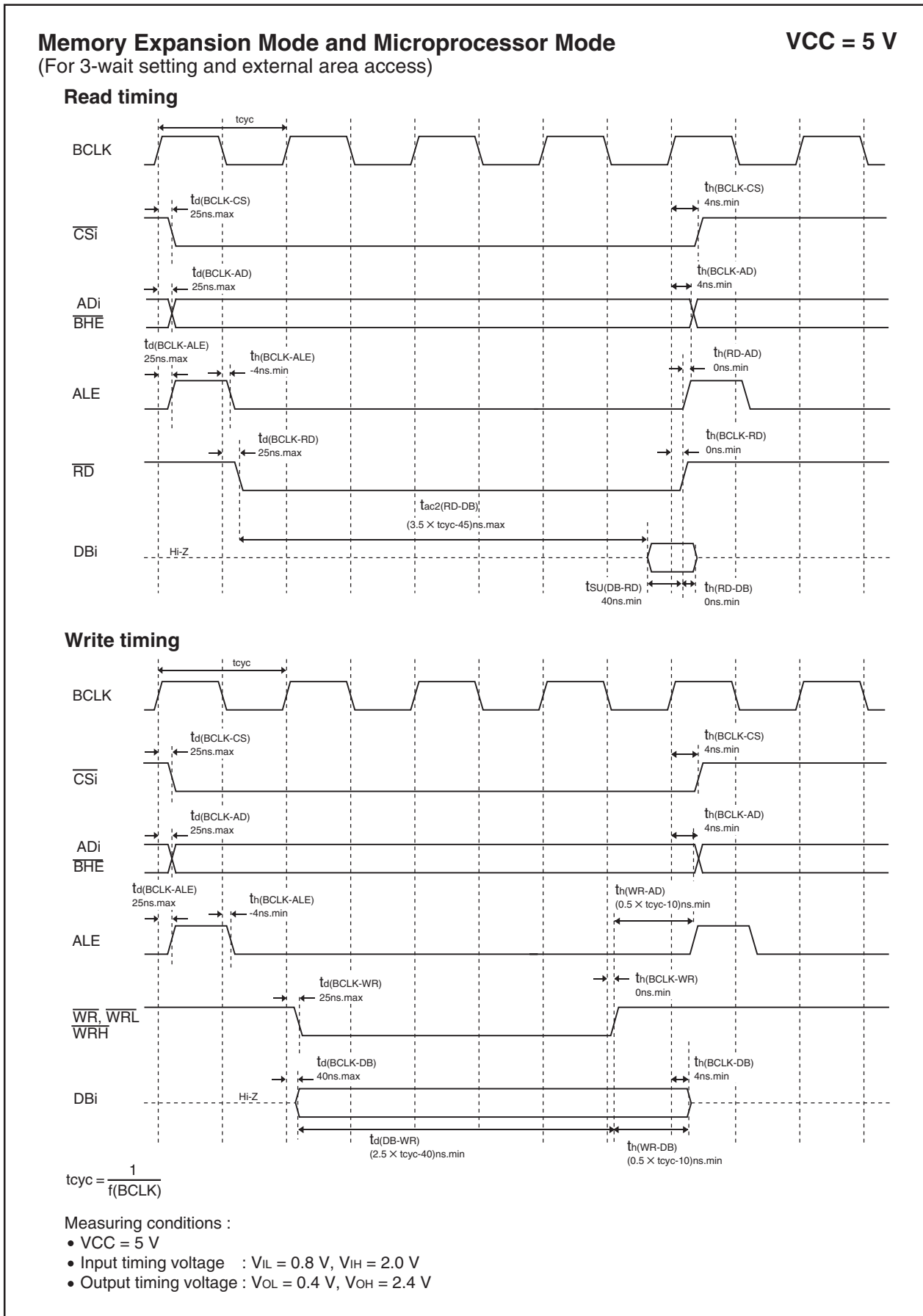


Figure 5.8 Timing Diagram (6)

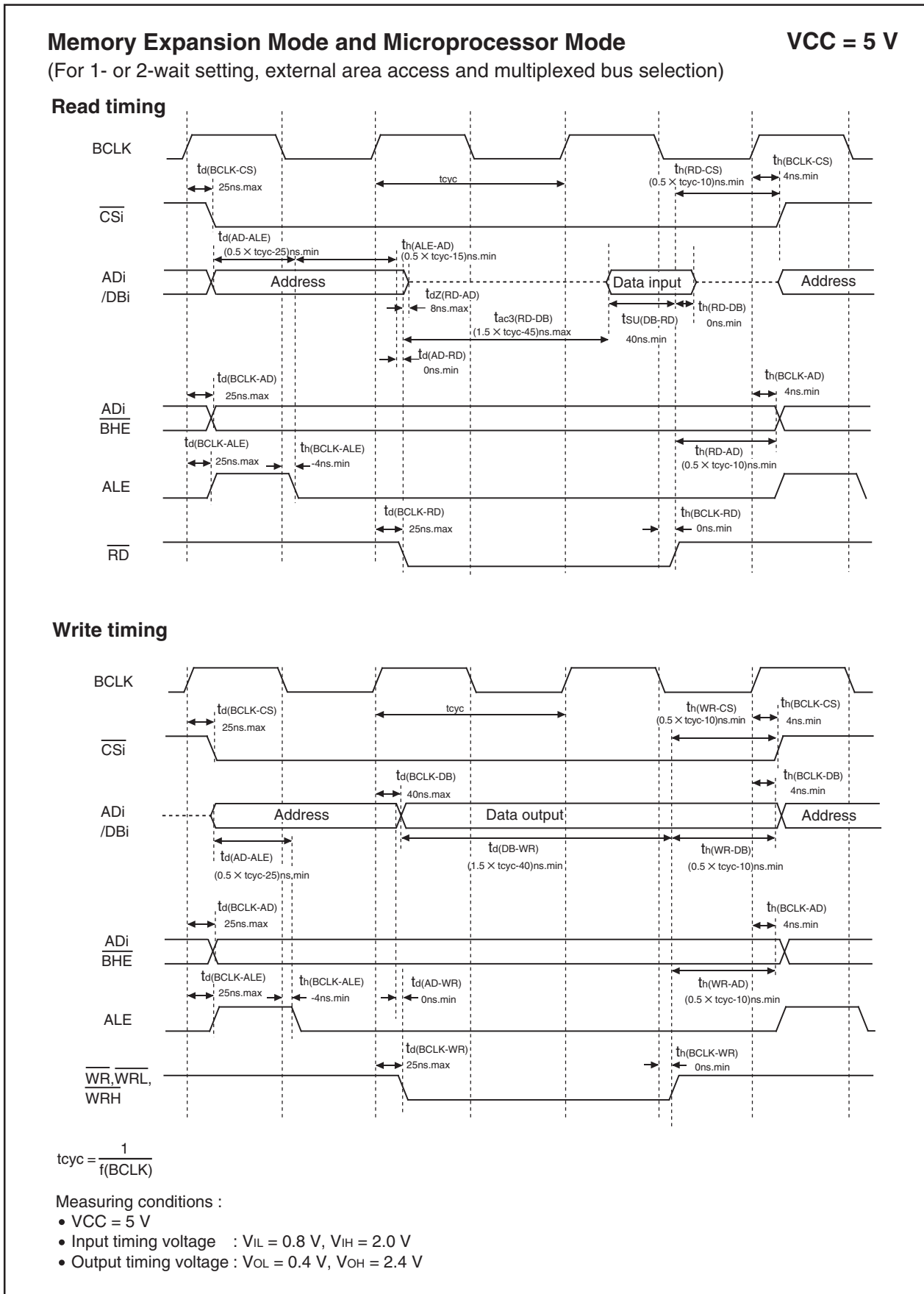


Figure 5.9 Timing Diagram (7)

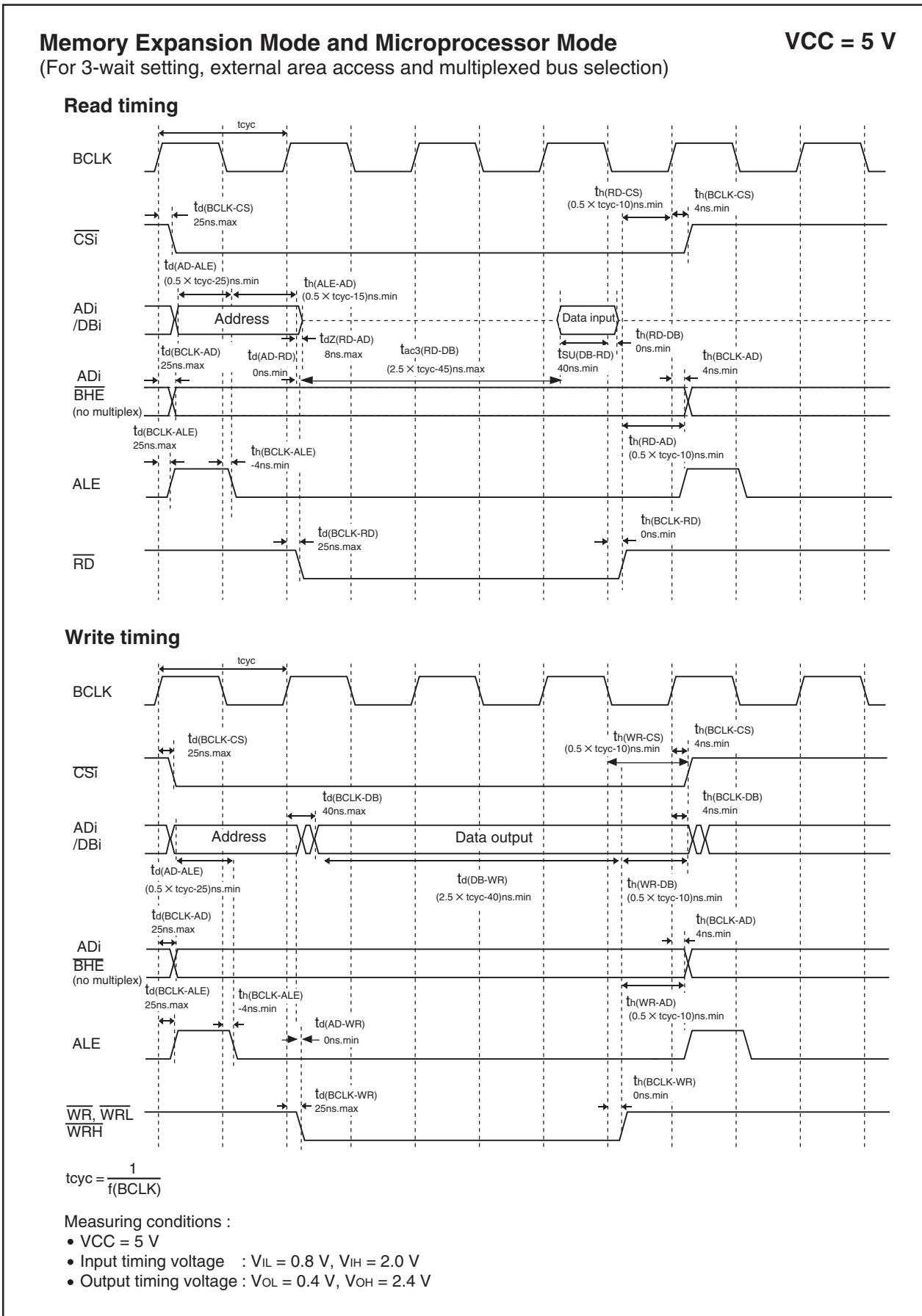


Figure 5.10 Timing Diagram (8)

5.2 Electrical Characteristics (Normal-ver.)

Table 5.26 Absolute Maximum Ratings

| Symbol | Parameter | | Condition | Rated Value | Unit |
|------------------|-------------------------------|--|-------------------------|-----------------|------|
| V _{CC} | Supply voltage (VCC1 = VCC2) | | VCC = AVCC | -0.3 to 6.5 | V |
| AV _{CC} | Analog supply voltage | | VCC = AVCC | -0.3 to 6.5 | V |
| V _i | Input voltage | RESET, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, VREF, XIN | | -0.3 to VCC+0.3 | V |
| | | P7_1, P9_1 | | -0.3 to 6.5 | V |
| V _o | Output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XOUT | | -0.3 to VCC+0.3 | V |
| | | P7_1, P9_1 | | -0.3 to 6.5 | V |
| P _d | Power dissipation | | T _{opr} = 25°C | 700 | mW |
| T _{opr} | Operating ambient temperature | During MCU operation | | -40 to 85 | °C |
| | | During flash memory program and erase operation | | 0 to 60 | |
| T _{stg} | Storage temperature | | | -65 to 150 | °C |

Table 5.27 Recommended Operating Conditions (1) ⁽¹⁾

| Symbol | Parameter | | Standard | | | Unit |
|-----------------------|---|--|---------------------|-----------------|----------------------|------|
| | | | Min. | Typ. | Max. | |
| V _{CC} | Supply voltage (V _{CC1} = V _{CC2}) | | 3.0 | 5.0 | 5.5 | V |
| AV _{CC} | Analog supply voltage | | | V _{CC} | | V |
| V _{SS} | Supply voltage | | | 0 | | V |
| AV _{SS} | Analog supply voltage | | | 0 | | V |
| V _{IH} | HIGH input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | 0.8 V _{CC} | | V _{CC} | V |
| | | P7_1, P9_1 | 0.8 V _{CC} | | 6.5 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode) | 0.8 V _{CC} | | V _{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes) | 0.5 V _{CC} | | V _{CC} | V |
| V _{IL} | LOW input voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | 0 | | 0.2 V _{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode) | 0 | | 0.2 V _{CC} | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes) | 0 | | 0.16 V _{CC} | V |
| I _{OH(peak)} | HIGH peak output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | | | -10.0 | mA |
| I _{OH(avg)} | HIGH average output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | | | -5.0 | mA |
| I _{OL(peak)} | LOW peak output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | 10.0 | mA |
| I _{OL(avg)} | LOW average output current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | | | 5.0 | mA |

NOTES:

1. Referenced to V_{CC} = 3.0 to 5.5 V at T_{opr} = -40 to 85°C unless otherwise specified.
2. Average output current values during 100 ms period.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9, and P10 must be 80 mA max.
The total I_{OL(peak)} for ports P3, P4, P5, P6, P7, and P8_0 to P8_4 must be 80 mA max.
The total I_{OH(peak)} for ports P0, P1, and P2 must be -40 mA max.
The total I_{OH(peak)} for ports P3, P4, and P5 must be -40 mA max.
The total I_{OH(peak)} for ports P6, P7, and P8_0 to P8_4 must be -40 mA max.
The total I_{OH(peak)} for ports P8_6, P8_7, P9, and P10 must be -40 mA max.

Table 5.28 Recommended Operating Conditions (2) ⁽¹⁾

| Symbol | Parameter | | | | Standard | | | Unit |
|----------------------|---|---------|--|--------------------|----------|--------|------|------|
| | | | | | Min. | Typ. | Max. | |
| f(XIN) | Main clock input oscillation frequency ^{(2) (3) (4)} | No wait | Mask ROM version Flash memory version | VCC = 3.0 to 5.5 V | 0 | | 16 | MHz |
| f(XCIN) | Sub clock oscillation frequency | | | | | 32.768 | 50 | kHz |
| f(Ring) | On-chip oscillation frequency | | | | | 1 | | MHz |
| f(PLL) | PLL clock oscillation frequency | | | | 16 | | 24 | MHz |
| f(BCLK) | CPU operation clock | | | VCC = 3.0 to 5.5 V | 0 | | 24 | MHz |
| t _{su(PLL)} | PLL frequency synthesizer stabilization wait time | | | | | | 20 | ms |

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V at Topr = -40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency and supply voltage is shown right.
3. Execute program/erase of flash memory by VCC = 3.3 ± 0.3 V or VCC = 5.0 ± 0.5 V.
4. When using over 16 MHz, use PLL clock. PLL clock oscillation frequency which can be used is 16 MHz, 20 MHz or 24 MHz.

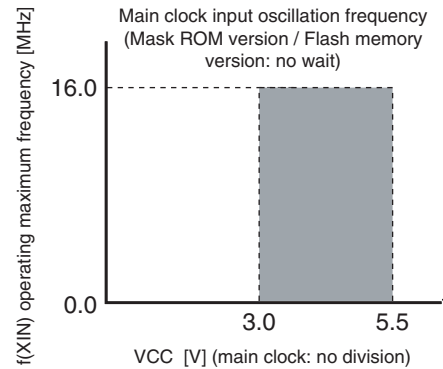


Table 5.29 A/D Conversion Characteristics ⁽¹⁾

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---------------------|--|---------|----------------------------------|---|----------|------|------------------|------|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | VREF = VCC | | | | 10 | Bit |
| INL | Integral nonlinearity error | 10 bits | VREF = VCC = 5 V | ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8 bits | VREF = AVCC = VCC = 5.0 V, 3.3 V | ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | | | ±5 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| – | Absolute accuracy | 10 bits | VREF = VCC = 5 V | ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8 bits | VREF = AVCC = VCC = 5.0 V, 3.3 V | ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input | | | ±5 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| DNL | Differential nonlinearity error | | VREF = AVCC = VCC = 5.0 V, 3.3 V | | | | ±1 | LSB |
| – | Offset error | | VREF = AVCC = VCC = 5.0 V, 3.3 V | | | | ±3 | LSB |
| – | Gain error | | VREF = AVCC = VCC = 5.0 V, 3.3 V | | | | ±3 | LSB |
| R _{LADDER} | Resistor ladder | | VREF = VCC | | 10 | | 40 | kΩ |
| t _{CONV} | 10-bit conversion time, sample & hold available | | VREF = VCC = 5 V, φAD = 10 MHz | | 3.3 | | | μs |
| | 8-bit conversion time, sample & hold available | | VREF = VCC = 5 V, φAD = 10 MHz | | 2.8 | | | μs |
| t _{SAMP} | Sampling time | | VREF = VCC = 5 V, φAD = 10 MHz | | 0.3 | | | μs |
| V _{REF} | Reference voltage | | VREF = VCC = 5 V, φAD = 10 MHz | | 2.0 | | V _{CC} | V |
| V _{IA} | Analog input voltage | | VREF = VCC = 5 V, φAD = 10 MHz | | 0 | | V _{REF} | V |

NOTES:

1. Referenced to VCC = AVCC = VREF = 3.3 to 5.5 V, VSS = AVSS = 0 V, –40 to 85°C unless otherwise specified.
2. φAD frequency must be 10 MHz or less.
3. When sample & hold is disabled, φAD frequency must be 250 kHz or more in addition to a limit of NOTE 2.
When sample & hold is enabled, φAD frequency must be 1 MHz or more in addition to a limit of NOTE 2.

Table 5.30 D/A conversion Characteristics ⁽¹⁾

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|-------------------|--------------------------------------|---------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy | | | | 1.0 | % |
| t _{su} | Setup time | | | | 3 | μs |
| R _o | Output resistance | | 4 | 10 | 20 | kΩ |
| I _{VREF} | Reference power supply input current | (NOTE 2) | | | 1.5 | mA |

NOTES:

1. Referenced to VCC = AVCC = VREF = 3.3 to 5.5 V, VSS = AVSS = 0 V, –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to 00h.
The resistor ladder of the A/D converter is not included. Also, the current I_{VREF} always flows even though VREF may have been set to be unconnected by the ADCON1 register.

Table 5.31 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|--------------|---|---------------------|----------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during powering-on | VCC = 3.0 to 5.5 V | | | 2 | ms |
| $t_{d(R-S)}$ | STOP release time | | | | 150 | μ s |
| $t_{d(W-S)}$ | Low power dissipation mode wait mode release time | | | | 150 | μ s |

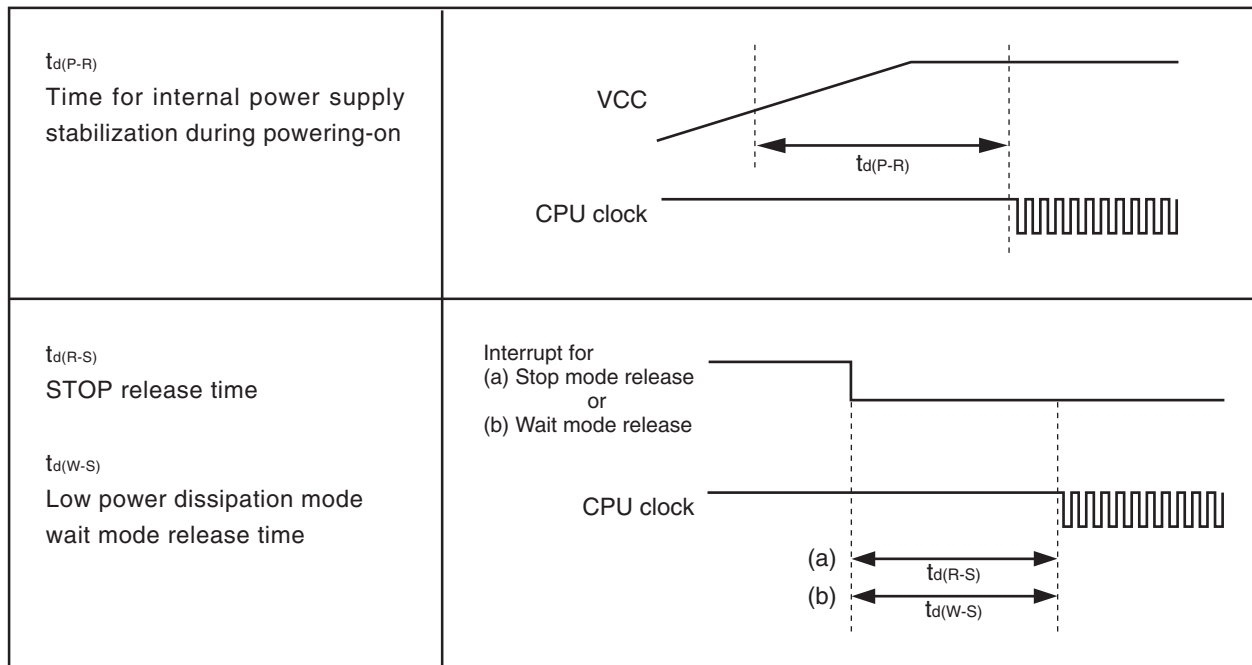


Figure 5.11 Power Supply Circuit Timing Diagram

Table 5.32 Electrical Characteristics (1) ⁽¹⁾

VCC = 5 V

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|----------------------------------|-----------------------|--|---------------------------|---------------------------|------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | HIGH output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | I _{OH} = -5 mA | V _{CC} -2.0 | | V _{CC} | V |
| V _{OH} | HIGH output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | I _{OH} = -200 μA | V _{CC} -0.3 | | V _{CC} | V |
| V _{OH} | HIGH output voltage | XOUT | HIGHPOWER | I _{OH} = -1 mA | 3.0 | V _{CC} | V |
| | | | LOWPOWER | I _{OH} = -0.5 mA | 3.0 | V _{CC} | |
| | HIGH output voltage | XCOUT | HIGHPOWER | With no load applied | | 2.5 | V |
| | | | LOWPOWER | With no load applied | | 1.6 | |
| V _{OL} | LOW output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | I _{OL} = 5 mA | | | 2.0 | V |
| V _{OL} | LOW output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | I _{OL} = 200 μA | | | 0.45 | V |
| V _{OL} | LOW output voltage | XOUT | HIGHPOWER | I _{OL} = 1 mA | | 2.0 | V |
| | | | LOWPOWER | I _{OL} = 0.5 mA | | 2.0 | |
| | LOW output voltage | XCOUT | HIGHPOWER | With no load applied | | 0 | V |
| | | | LOWPOWER | With no load applied | | 0 | |
| V _{T+} -V _{T-} | Hysteresis | HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, $\overline{KI}0$ to $\overline{KI}3$, RXD0 to RXD2, SIN3 | | 0.2 | | 1.0 | V |
| V _{T+} -V _{T-} | Hysteresis | RESET | | 0.2 | | 2.5 | V |
| I _{IH} | HIGH input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | V _I = 5 V | | | 5.0 | μA |
| I _{IL} | LOW input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, \overline{RESET} , CNVSS, BYTE | V _I = 0 V | | | -5.0 | μA |
| R _{PULLUP} | Pull-up resistance | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | V _I = 0 V | 30 | 50 | 170 | kΩ |
| R _{FXIN} | Feedback resistance | XIN | | | 1.5 | | MΩ |
| R _{FXCIN} | Feedback resistance | XCIN | | | 15 | | MΩ |
| V _{RAM} | RAM retention voltage | | At stop mode | 2.0 | | | V |

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.

Table 5.33 Electrical Characteristics (2) ⁽¹⁾

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|-----------------|--|---|----------------------|---|--------------------------------|------|------|------|
| | | | | | Min. | Typ. | Max. | |
| I _{cc} | Power supply current (VCC = 3.0 to 5.5 V) | In single-chip mode, the output pins are open and other pins are VSS. | Mask ROM | f(BCLK) = 24 MHz, PLL operation, No division | | 20 | 36 | mA |
| | | | | On-chip oscillation, No division | | 1 | | mA |
| | | | Flash memory | f(BCLK) = 24 MHz, PLL operation, No division | | 22 | 38 | mA |
| | | | | On-chip oscillation, No division | | 1.8 | | mA |
| | | | Flash memory program | f(BCLK) = 10 MHz, VCC = 5 V | | 15 | | mA |
| | | | Flash memory erase | f(BCLK) = 10 MHz, VCC = 5 V | | 25 | | mA |
| | | | Mask ROM | f(BCLK) = 32 kHz, Low power dissipation mode, ROM ⁽²⁾ | | 25 | | μA |
| | | | Flash memory | f(BCLK) = 32 kHz, Low power dissipation mode, RAM ⁽²⁾ | | 25 | | μA |
| | | | | f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory ⁽²⁾ | | 420 | | μA |
| | | | | Mask ROM Flash memory | On-chip oscillation, Wait mode | | 50 | |
| | | | Flash memory | f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity High | | 8.5 | | μA |
| | | | | f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity Low | | 3.0 | | μA |
| | | | | Stop mode, Topr = 25°C | | 0.8 | 3.0 | μA |

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V, VSS = 0 V at Topr = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.34 External Clock Input (XIN Input)**

| Symbol | Parameter | Standard | | Unit |
|-------------------|---------------------------------------|----------|------|------|
| | | Min. | Max. | |
| t _c | External clock input cycle time | 62.5 | | ns |
| t _{w(H)} | External clock input HIGH pulse width | 25 | | ns |
| t _{w(L)} | External clock input LOW pulse width | 25 | | ns |
| t _r | External clock rise time | | 15 | ns |
| t _f | External clock fall time | | 15 | ns |

Table 5.35 Memory Expansion Mode and Microprocessor Mode

| Symbol | Parameter | Standard | | Unit |
|----------------------------|--|----------|----------|------|
| | | Min. | Max. | |
| t _{ac1(RD-DB)} | Data input access time (for setting with no wait) | | (NOTE 1) | ns |
| t _{ac2(RD-DB)} | Data input access time (for setting with wait) | | (NOTE 2) | ns |
| t _{ac3(RD-DB)} | Data input access time (when accessing multiplexed bus area) | | (NOTE 3) | ns |
| t _{su(DB-RD)} | Data input setup time | 40 | | ns |
| t _{su(RDY-BCLK)} | RDY input setup time | 30 | | ns |
| t _{su(HOLD-BCLK)} | HOLD input setup time | 40 | | ns |
| t _{h(RD-DB)} | Data input hold time | 0 | | ns |
| t _{h(BCLK-RDY)} | RDY input hold time | 0 | | ns |
| t _{h(BCLK-HOLD)} | HOLD input hold time | 0 | | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.36 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 40 | | ns |

Table 5.37 Timer A Input (Gating Input in Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 200 | | ns |

Table 5.38 Timer A Input (External Trigger Input in One-shot Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 100 | | ns |

Table 5.39 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 100 | | ns |

Table 5.40 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|------------------|-------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT input cycle time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT input HIGH pulse width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT input LOW pulse width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT input setup time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT input hold time | 400 | | ns |

Table 5.41 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|----------------------|-------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT input setup time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN input setup time | 200 | | ns |

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.42 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|--------------|--|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on both edges) | 80 | | ns |

Table 5.43 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width | 200 | | ns |

Table 5.44 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width | 200 | | ns |

Table 5.45 A/D Trigger Input

| Symbol | Parameter | Standard | | Unit |
|--------------|---|----------|------|------|
| | | Min. | Max. | |
| $t_{c(AD)}$ | ADTRG input cycle time (trigger able minimum) | 1000 | | ns |
| $t_{w(ADL)}$ | ADTRG input LOW pulse width | 125 | | ns |

Table 5.46 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input HIGH pulse width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi input LOW pulse width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | | ns |

Table 5.47 External Interrupt INTi Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | INTi input HIGH pulse width | 250 | | ns |
| $t_{w(INL)}$ | INTi input LOW pulse width | 250 | | ns |

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Table 5.48 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|--|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.12 | | 25 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | 0 | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 25 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (BCLK-ALE) | ALE signal output delay time | | | 15 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time | | -4 | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 25 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 25 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) ⁽³⁾ | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) ⁽³⁾ | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | 40 | ns | |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad f(\text{BCLK}) \text{ is } 12.5 \text{ MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF,

R = 1 kΩ, hold time of output "L" level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$

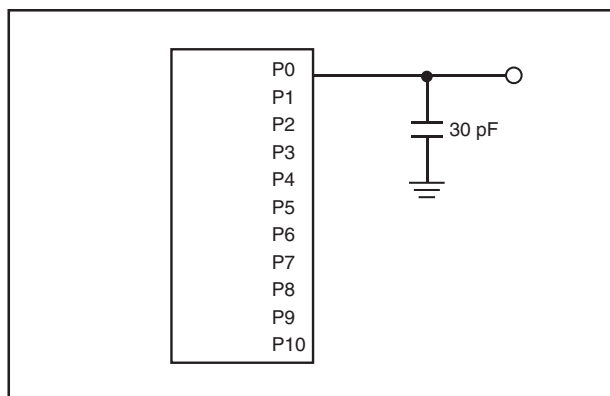
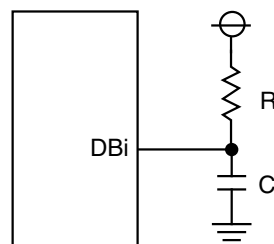


Figure 5.12 Port P0 to P10 Measurement Circuit

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Table 5.49 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|--|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.12 | | 25 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | 0 | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 25 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (BCLK-ALE) | ALE signal output delay time | | | 15 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time | | -4 | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 25 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 25 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) ⁽³⁾ | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) ⁽³⁾ | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | 40 | ns | |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

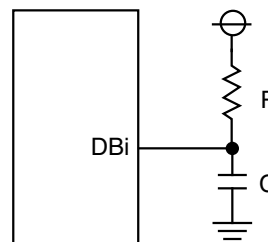
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF,

R = 1 kΩ, hold time of output "L" level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$



Switching Characteristics**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.50 Memory Expansion Mode and Microprocessor Mode
(for 2- to 3-wait setting, external area access and multiplexed bus selection)**

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|---|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.12 | | 25 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | (NOTE 1) | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 25 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-CS) | Chip select output hold time (in relation to RD) | | (NOTE 1) | | ns |
| t _h (WR-CS) | Chip select output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 25 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 25 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | | 40 | ns |
| t _d (BCLK-ALE) | ALE signal output delay time (in relation to BCLK) | | | 15 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time (in relation to BCLK) | | –4 | | ns |
| t _d (AD-ALE) | ALE signal output delay time (in relation to Address) | | (NOTE 3) | | ns |
| t _h (ALE-AD) | ALE signal output hold time (in relation to Address) | | (NOTE 4) | | ns |
| t _d (AD-RD) | RD signal output delay from the end of Address | | 0 | | ns |
| t _d (AD-WR) | WR signal output delay from the end of Address | | 0 | | ns |
| t _{dZ} (RD-AD) | Address output floating start time | | | 8 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 \text{ [ns]}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \text{ [ns]}$$

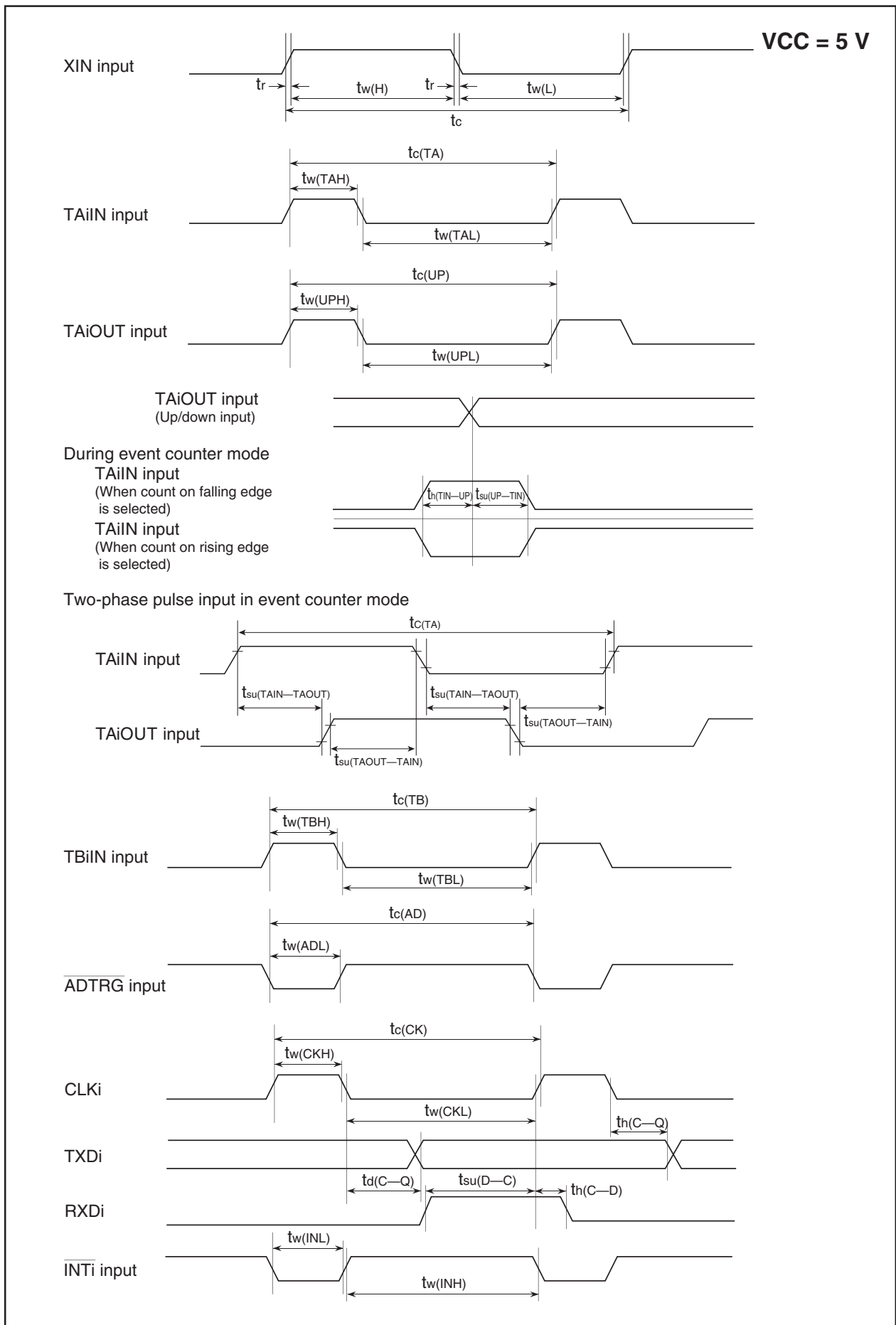


Figure 5.13 Timing Diagram (1)

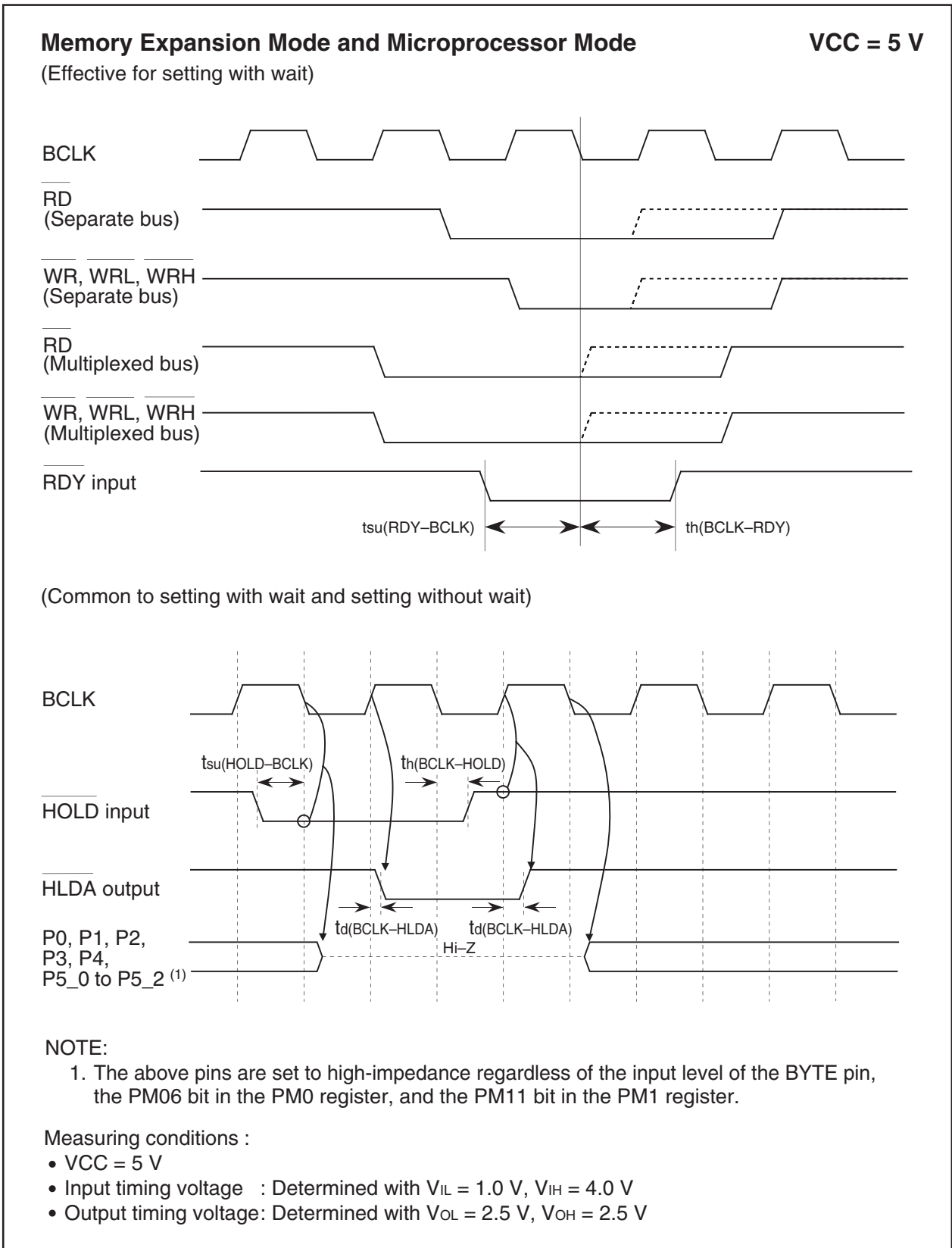


Figure 5.14 Timing Diagram (2)

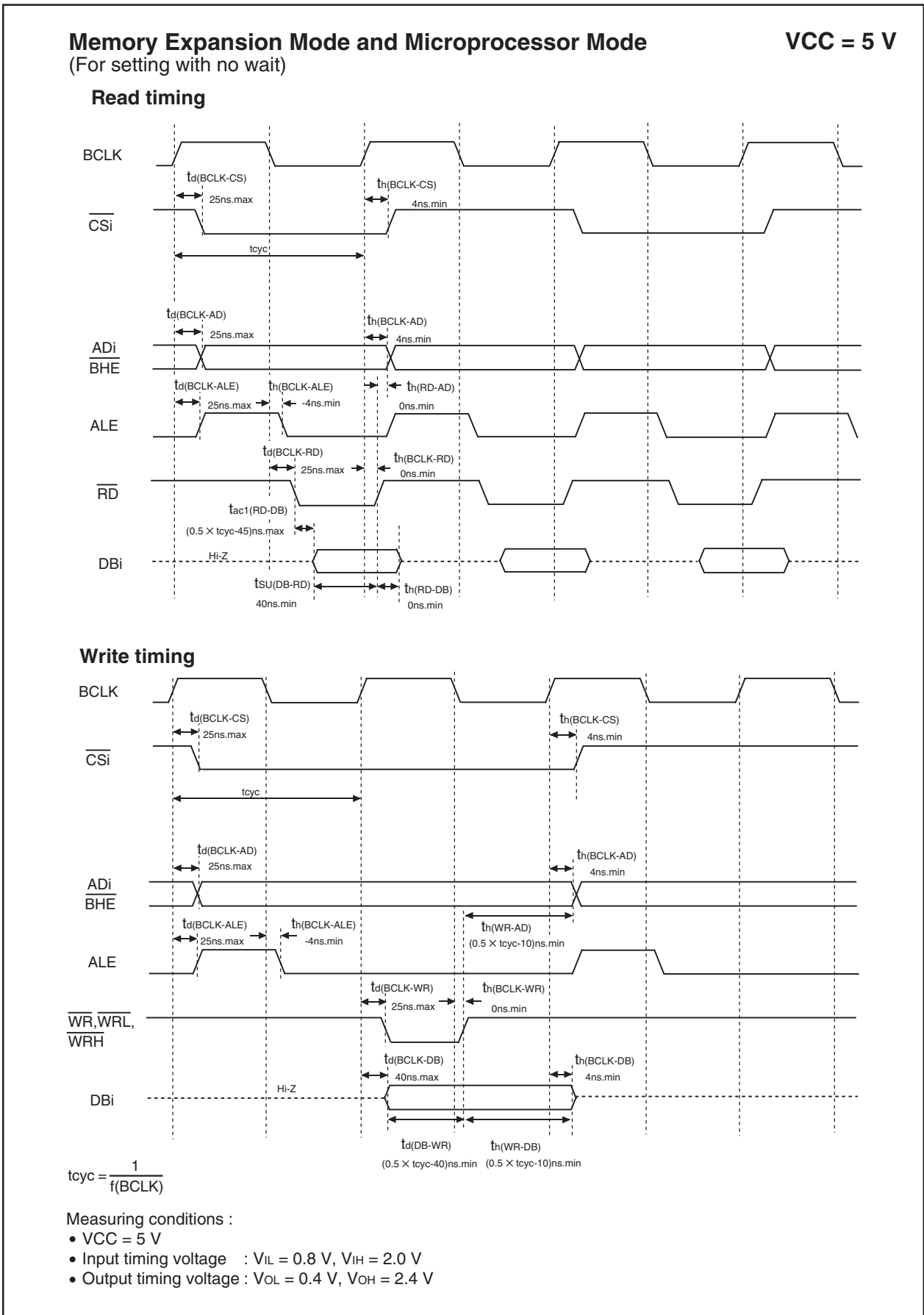


Figure 5.15 Timing Diagram (3)

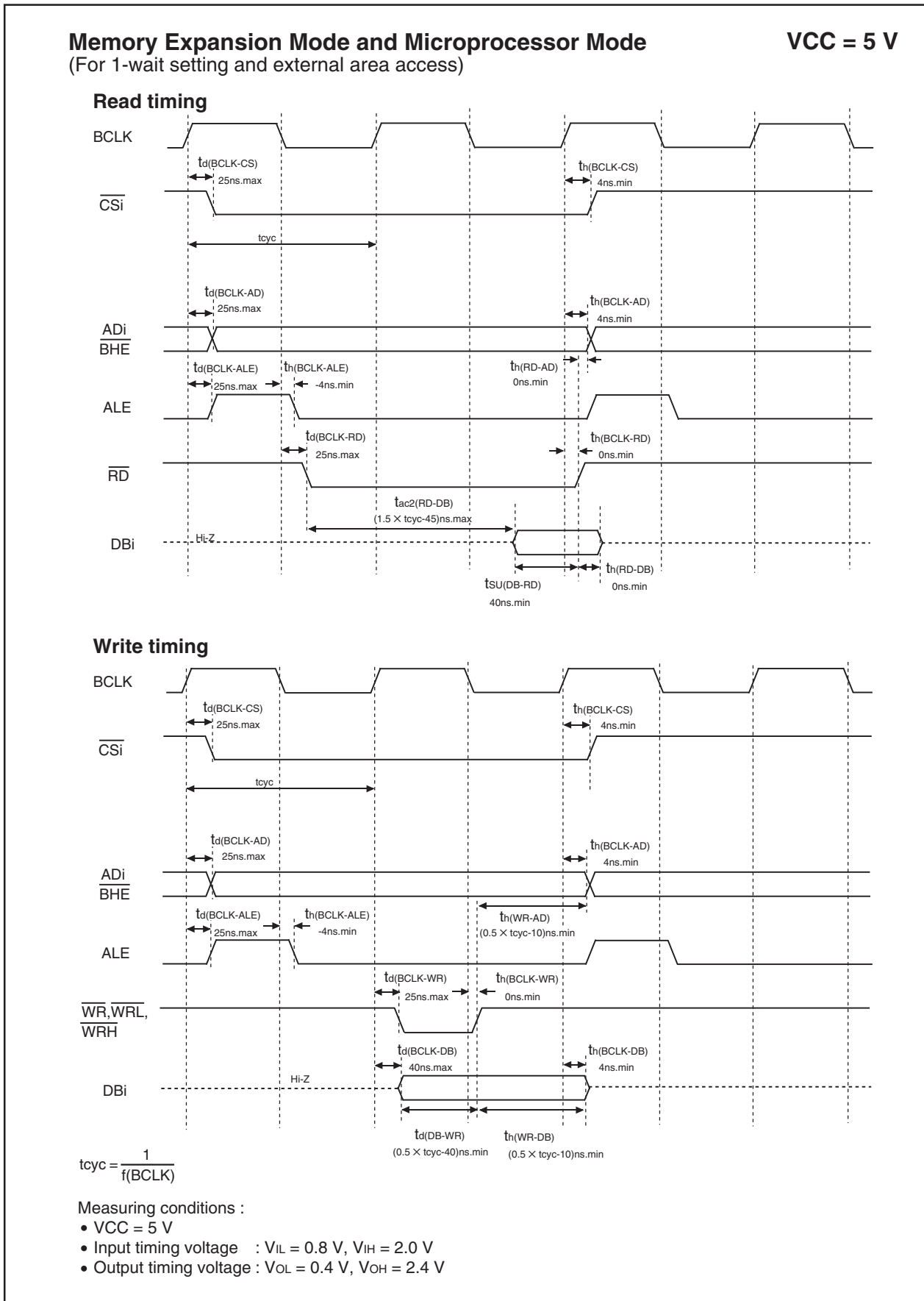


Figure 5.16 Timing Diagram (4)

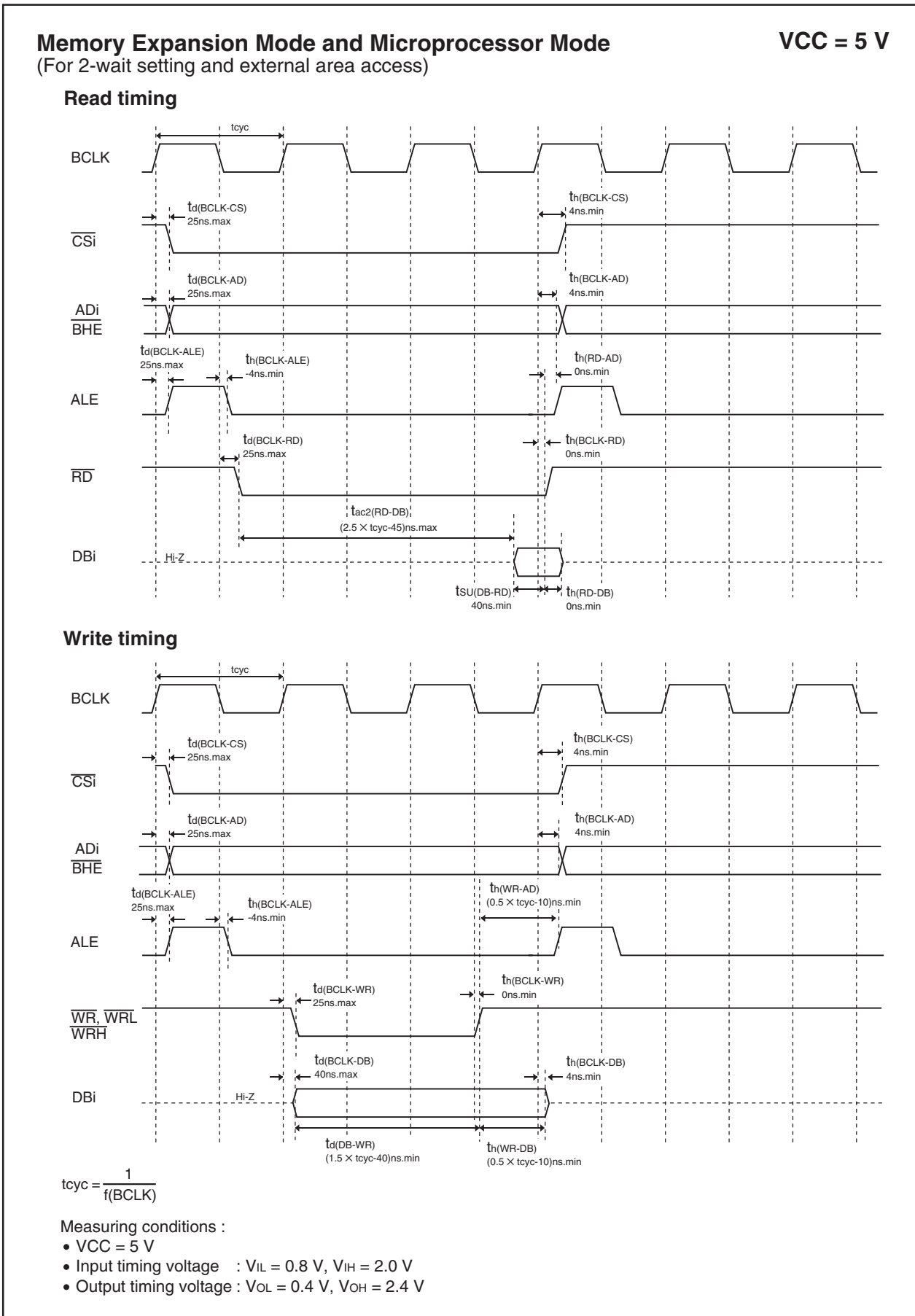


Figure 5.17 Timing Diagram (5)

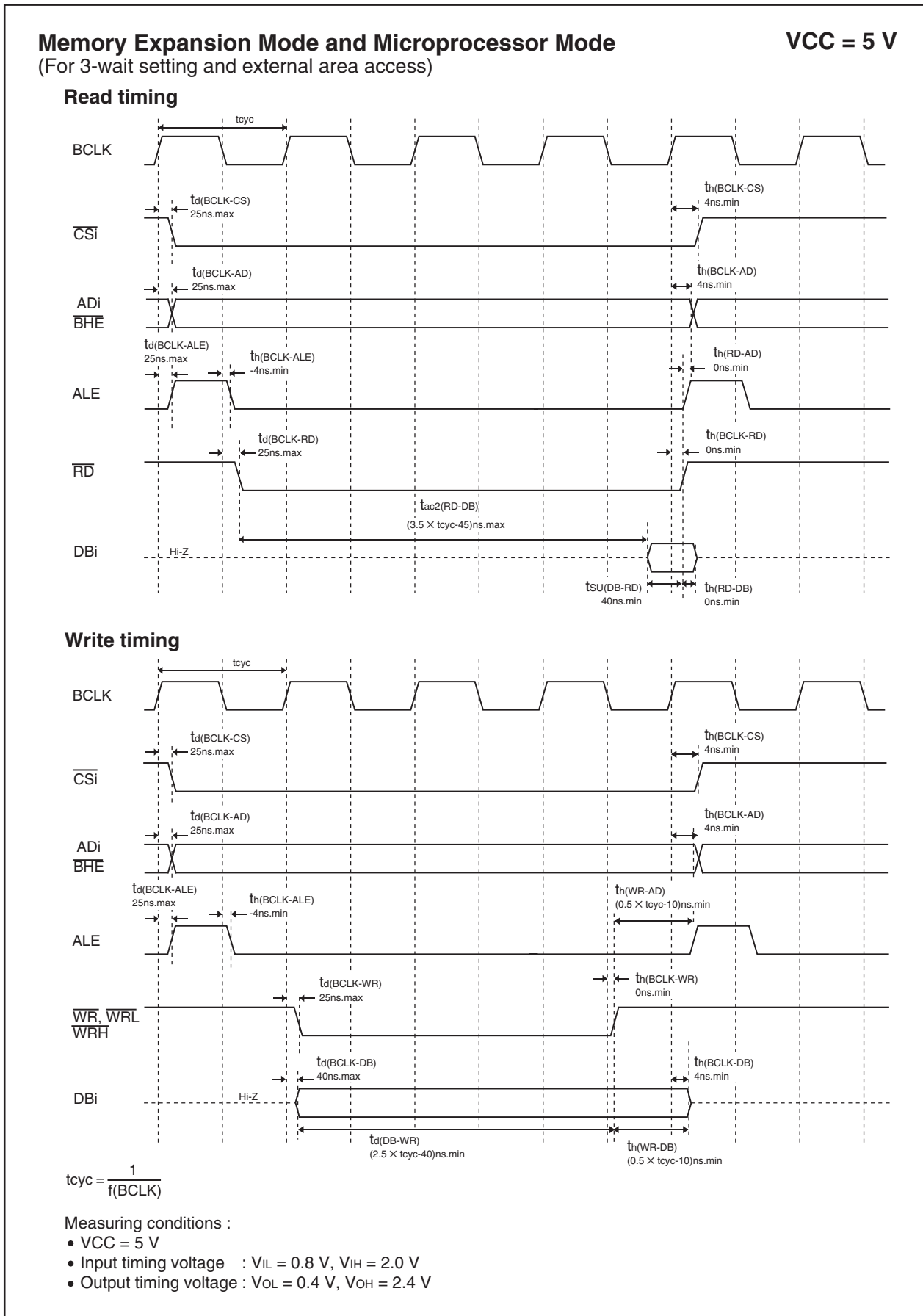


Figure 5.18 Timing Diagram (6)

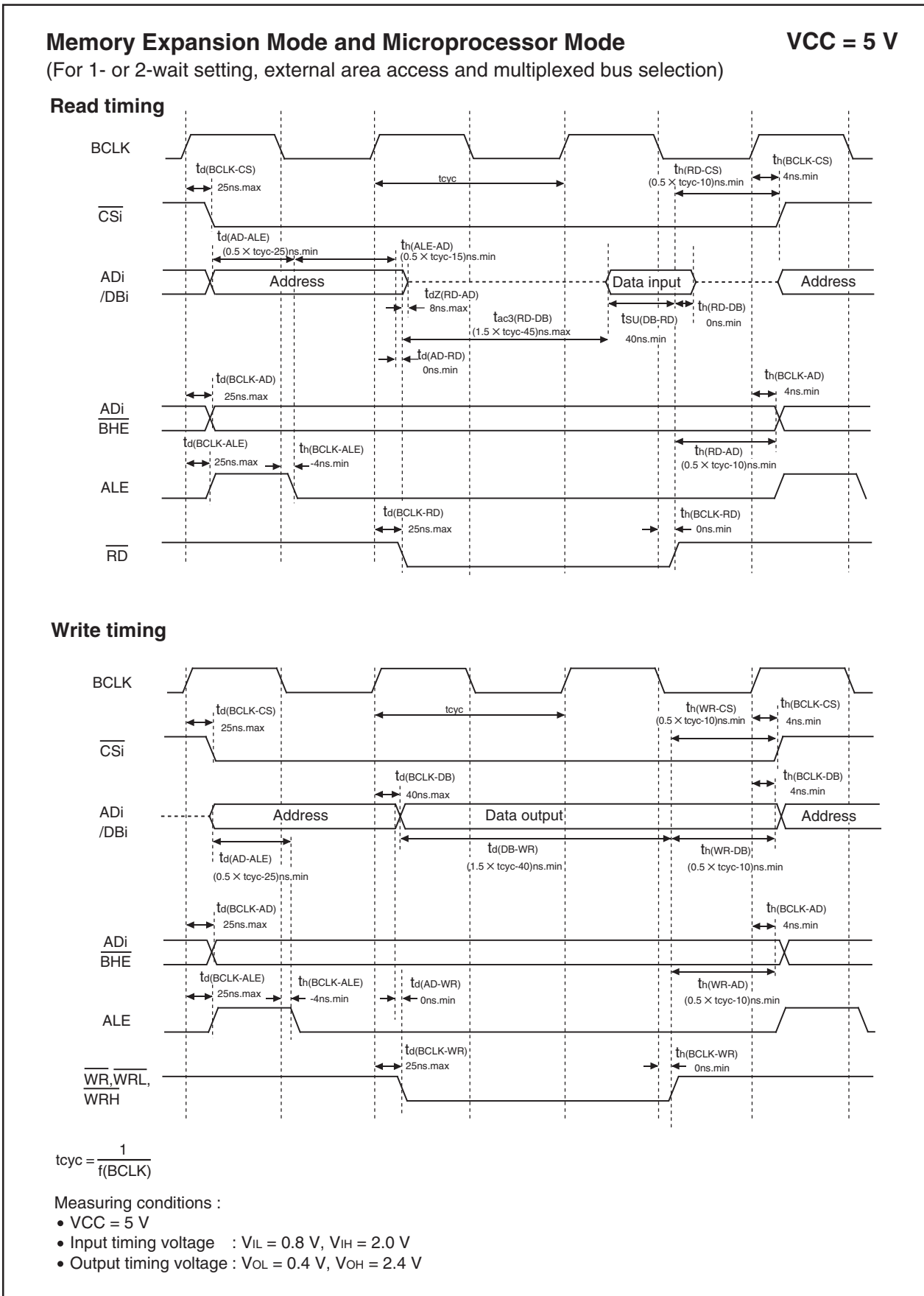


Figure 5.19 Timing Diagram (7)

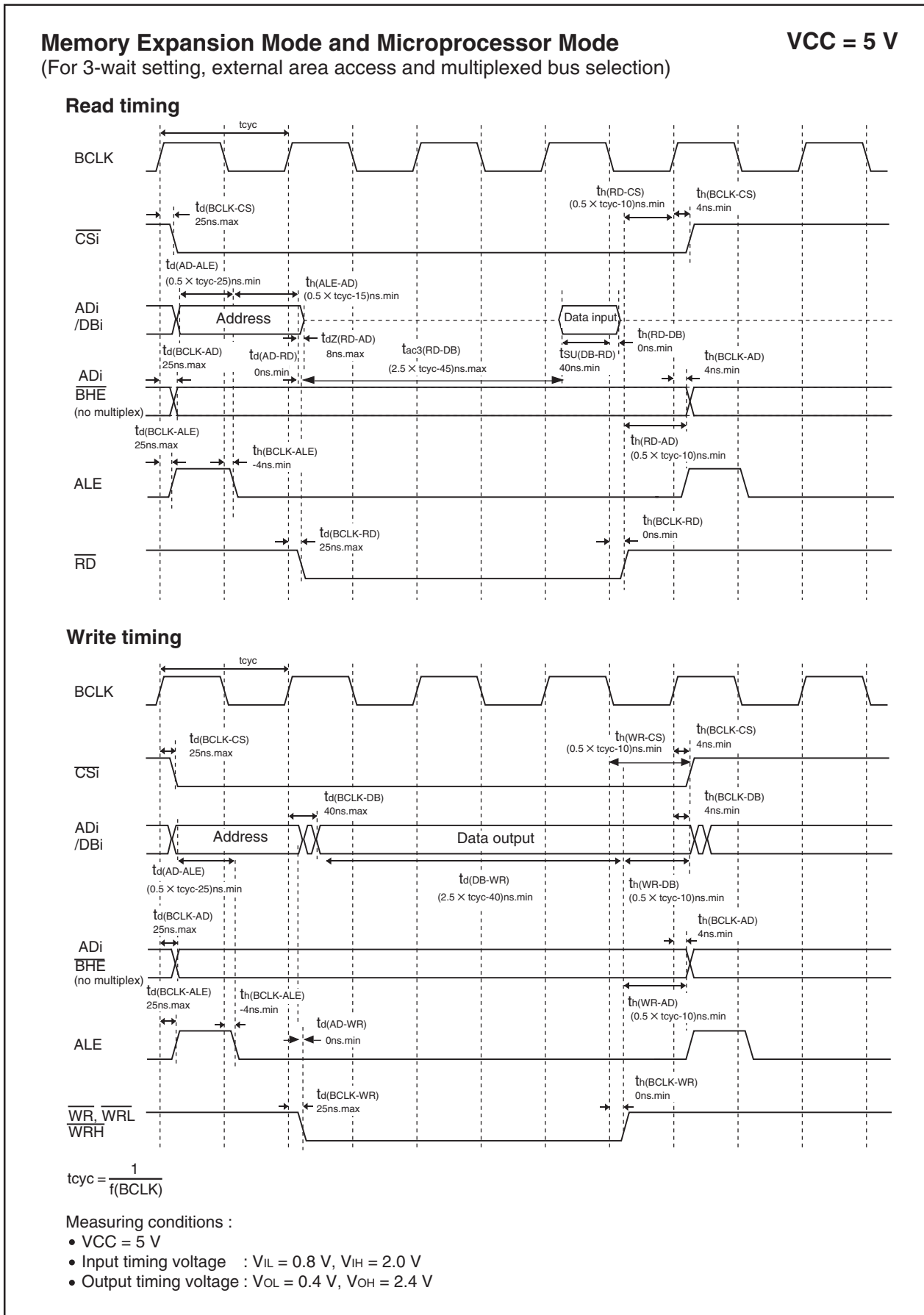


Figure 5.20 Timing Diagram (8)

Table 5.51 Electrical Characteristics ⁽¹⁾

VCC = 3.3 V

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|----------------------------------|-----------------------|---|-------------------------|---------------------------|----------------------|-----------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{OH} | HIGH output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | I _{OH} = -1 mA | V _{CC} -0.5 | | V _{CC} | V |
| V _{OH} | HIGH output voltage | XOUT | HIGHPOWER | I _{OH} = -0.1 mA | V _{CC} -0.5 | V _{CC} | V |
| | | | LOWPOWER | I _{OH} = -50 μA | V _{CC} -0.5 | V _{CC} | |
| | HIGH output voltage | XCOUT | HIGHPOWER | With no load applied | | 2.5 | V |
| | | | LOWPOWER | With no load applied | | 1.6 | |
| V _{OL} | LOW output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 | I _{OL} = 1 mA | | | 0.5 | V |
| V _{OL} | LOW output voltage | XOUT | HIGHPOWER | I _{OL} = 0.1 mA | | 0.5 | V |
| | | | LOWPOWER | I _{OL} = 50 μA | | 0.5 | |
| | LOW output voltage | XCOUT | HIGHPOWER | With no load applied | | 0 | V |
| | | | LOWPOWER | With no load applied | | 0 | |
| V _{T+} -V _{T-} | Hysteresis | HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SIN3 | | 0.2 | | 0.8 | V |
| V _{T+} -V _{T-} | Hysteresis | RESET | | 0.2 | | 1.8 | V |
| I _{IH} | HIGH input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | V _I = 3.3 V | | | 4.0 | μA |
| I _{IL} | LOW input current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE | V _I = 0 V | | | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7 | V _I = 0 V | 50 | 100 | 500 | kΩ |
| R _{IXIN} | Feedback resistance | XIN | | | 3.0 | | MΩ |
| R _{IXCIN} | Feedback resistance | XCIN | | | 25 | | MΩ |
| V _{RAM} | RAM retention voltage | | At stop mode | 2.0 | | | V |

NOTES:

1. Referenced to VCC = 3.0 to 3.6 V, VSS = 0 V at Topr = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.

Timing Requirements**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.52 External Clock Input (XIN Input)**

| Symbol | Parameter | Standard | | Unit |
|-------------------|---------------------------------------|----------|------|------|
| | | Min. | Max. | |
| t _c | External clock input cycle time | 62.5 | | ns |
| t _{w(H)} | External clock input HIGH pulse width | 25 | | ns |
| t _{w(L)} | External clock input LOW pulse width | 25 | | ns |
| t _r | External clock rise time | | 15 | ns |
| t _f | External clock fall time | | 15 | ns |

Table 5.53 Memory Expansion Mode and Microprocessor Mode

| Symbol | Parameter | Standard | | Unit |
|----------------------------|--|----------|----------|------|
| | | Min. | Max. | |
| t _{ac1(RD-DB)} | Data input access time (for setting with no wait) | | (NOTE 1) | ns |
| t _{ac2(RD-DB)} | Data input access time (for setting with wait) | | (NOTE 2) | ns |
| t _{ac3(RD-DB)} | Data input access time (when accessing multiplexed bus area) | | (NOTE 3) | ns |
| t _{su(DB-RD)} | Data input setup time | 50 | | ns |
| t _{su(RDY-BCLK)} | RDY input setup time | 40 | | ns |
| t _{su(HOLD-BCLK)} | HOLD input setup time | 50 | | ns |
| t _{h(RD-DB)} | Data input hold time | 0 | | ns |
| t _{h(BCLK-RDY)} | RDY input hold time | 0 | | ns |
| t _{h(BCLK-HOLD)} | HOLD input hold time | 0 | | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 60 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 60 \text{ [ns]} \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 60 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Timing Requirements**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.54 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 150 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 60 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 60 | | ns |

Table 5.55 Timer A Input (Gating Input in Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 600 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 300 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 300 | | ns |

Table 5.56 Timer A Input (External Trigger Input in One-shot Timer Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 300 | | ns |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 150 | | ns |

Table 5.57 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN input HIGH pulse width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN input LOW pulse width | 150 | | ns |

Table 5.58 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|------------------|-------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT input cycle time | 3000 | | ns |
| $t_{w(UPH)}$ | TAiOUT input HIGH pulse width | 1500 | | ns |
| $t_{w(UPL)}$ | TAiOUT input LOW pulse width | 1500 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT input setup time | 600 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT input hold time | 600 | | ns |

Table 5.59 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|----------------------|-------------------------|----------|------|---------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 2 | | μ s |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT input setup time | 500 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN input setup time | 500 | | ns |

Timing Requirements**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.60 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|--------------|--|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on one edge) | 150 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on one edge) | 60 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on one edge) | 60 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (counted on both edges) | 300 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on both edges) | 120 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on both edges) | 120 | | ns |

Table 5.61 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width | 300 | | ns |

Table 5.62 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|--------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input cycle time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width | 300 | | ns |

Table 5.63 A/D Trigger Input

| Symbol | Parameter | Standard | | Unit |
|--------------|---|----------|------|------|
| | | Min. | Max. | |
| $t_{c(AD)}$ | ADTRG input cycle time (trigger able minimum) | 1500 | | ns |
| $t_{w(ADL)}$ | ADTRG input LOW pulse width | 200 | | ns |

Table 5.64 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | | ns |
| $t_{w(CKH)}$ | CLKi input HIGH pulse width | 150 | | ns |
| $t_{w(CKL)}$ | CLKi input LOW pulse width | 150 | | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | | 160 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 100 | | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | | ns |

Table 5.65 External Interrupt INTi Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | INTi input HIGH pulse width | 380 | | ns |
| $t_{w(INL)}$ | INTi input LOW pulse width | 380 | | ns |

Switching Characteristics

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Table 5.66 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|--|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.21 | | 30 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | 0 | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 30 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (BCLK-ALE) | ALE signal output delay time | | | 25 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time | | -4 | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 30 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 30 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) ⁽³⁾ | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) ⁽³⁾ | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | 40 | ns | |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad f(\text{BCLK}) \text{ is } 12.5 \text{ MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF, R = 1 kΩ, hold time of output "L" level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$

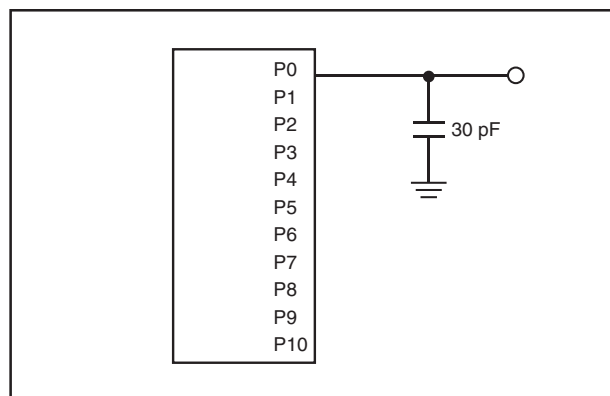
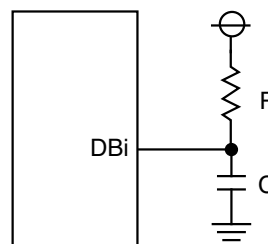


Figure 5.21 Port P0 to P10 Measurement Circuit

Switching Characteristics

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Table 5.67 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|--|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.21 | | 30 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | 0 | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 30 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (BCLK-ALE) | ALE signal output delay time | | | 25 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time | | -4 | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 30 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 30 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 40 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) ⁽³⁾ | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) ⁽³⁾ | (NOTE 1) | | ns | |
| t _d (BCLK-HLDA) | HLDA output delay time | | 40 | ns | |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

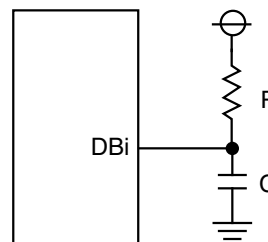
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF,

R = 1 kΩ, hold time of output "L" level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$



Switching Characteristics**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.68 Memory Expansion Mode and Microprocessor Mode
(for 2- to 3-wait setting, external area access and multiplexed bus selection)**

| Symbol | Parameter | Measuring Condition | Standard | | Unit |
|----------------------------|---|---------------------|----------|------|------|
| | | | Min. | Max. | |
| t _d (BCLK-AD) | Address output delay time | Figure 5.21 | | 50 | ns |
| t _h (BCLK-AD) | Address output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-AD) | Address output hold time (in relation to RD) | | (NOTE 1) | | ns |
| t _h (WR-AD) | Address output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-CS) | Chip select output delay time | | | 50 | ns |
| t _h (BCLK-CS) | Chip select output hold time (in relation to BCLK) | | 4 | | ns |
| t _h (RD-CS) | Chip select output hold time (in relation to RD) | | (NOTE 1) | | ns |
| t _h (WR-CS) | Chip select output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-RD) | RD signal output delay time | | | 40 | ns |
| t _h (BCLK-RD) | RD signal output hold time | | 0 | | ns |
| t _d (BCLK-WR) | WR signal output delay time | | | 40 | ns |
| t _h (BCLK-WR) | WR signal output hold time | | 0 | | ns |
| t _d (BCLK-DB) | Data output delay time (in relation to BCLK) | | | 50 | ns |
| t _h (BCLK-DB) | Data output hold time (in relation to BCLK) | | 4 | | ns |
| t _d (DB-WR) | Data output delay time (in relation to WR) | | (NOTE 2) | | ns |
| t _h (WR-DB) | Data output hold time (in relation to WR) | | (NOTE 1) | | ns |
| t _d (BCLK-HLDA) | HLDA output delay time | | | 40 | ns |
| t _d (BCLK-ALE) | ALE signal output delay time (in relation to BCLK) | | | 25 | ns |
| t _h (BCLK-ALE) | ALE signal output hold time (in relation to BCLK) | | –4 | | ns |
| t _d (AD-ALE) | ALE signal output delay time (in relation to Address) | | (NOTE 3) | | ns |
| t _h (ALE-AD) | ALE signal output hold time (in relation to Address) | | (NOTE 4) | | ns |
| t _d (AD-RD) | RD signal output delay from the end of Address | | 0 | | ns |
| t _d (AD-WR) | WR signal output delay from the end of Address | | 0 | | ns |
| t _{dZ} (RD-AD) | Address output floating start time | | | 8 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 50 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \text{ [ns]}$$

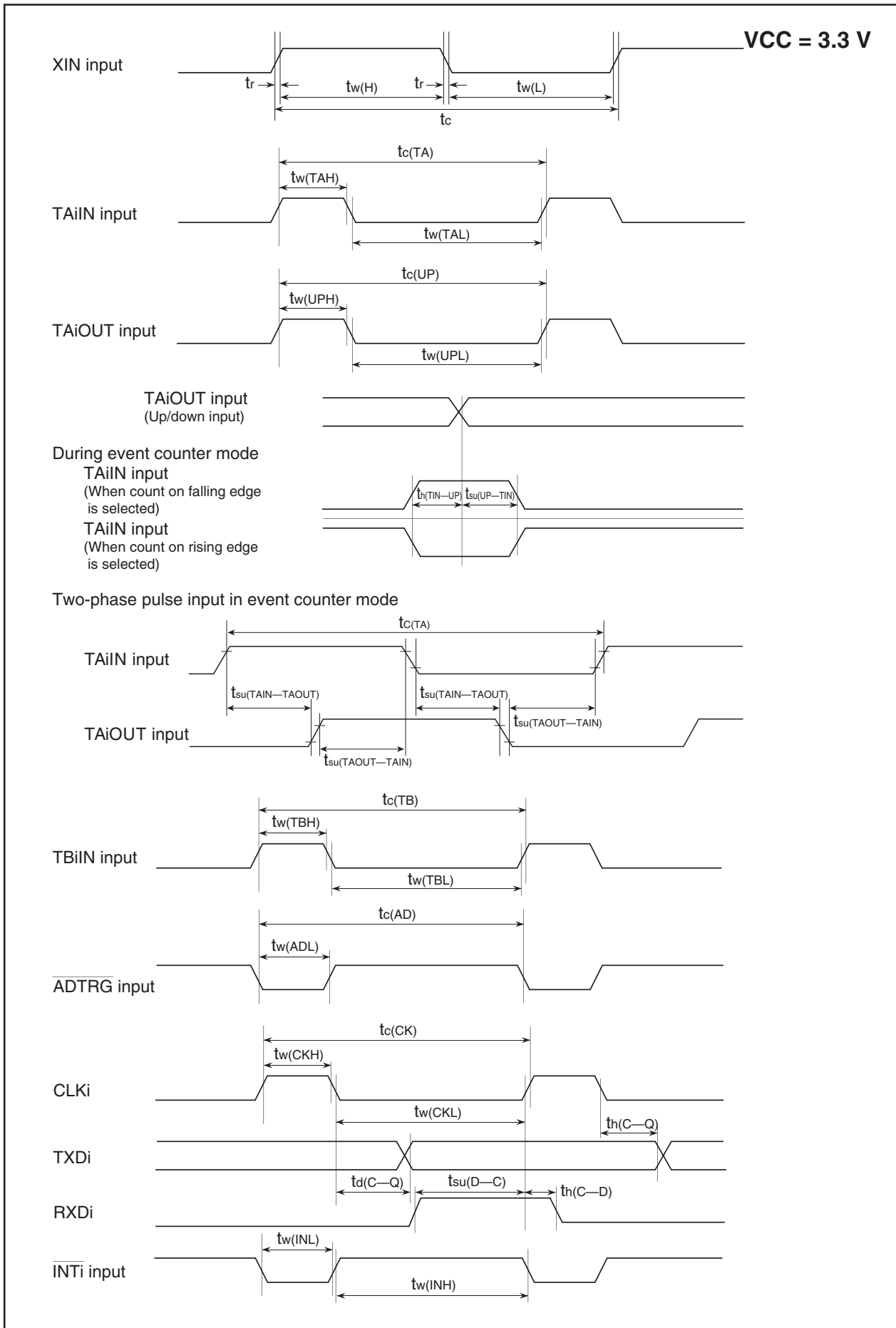


Figure 5.22 Timing Diagram (1)

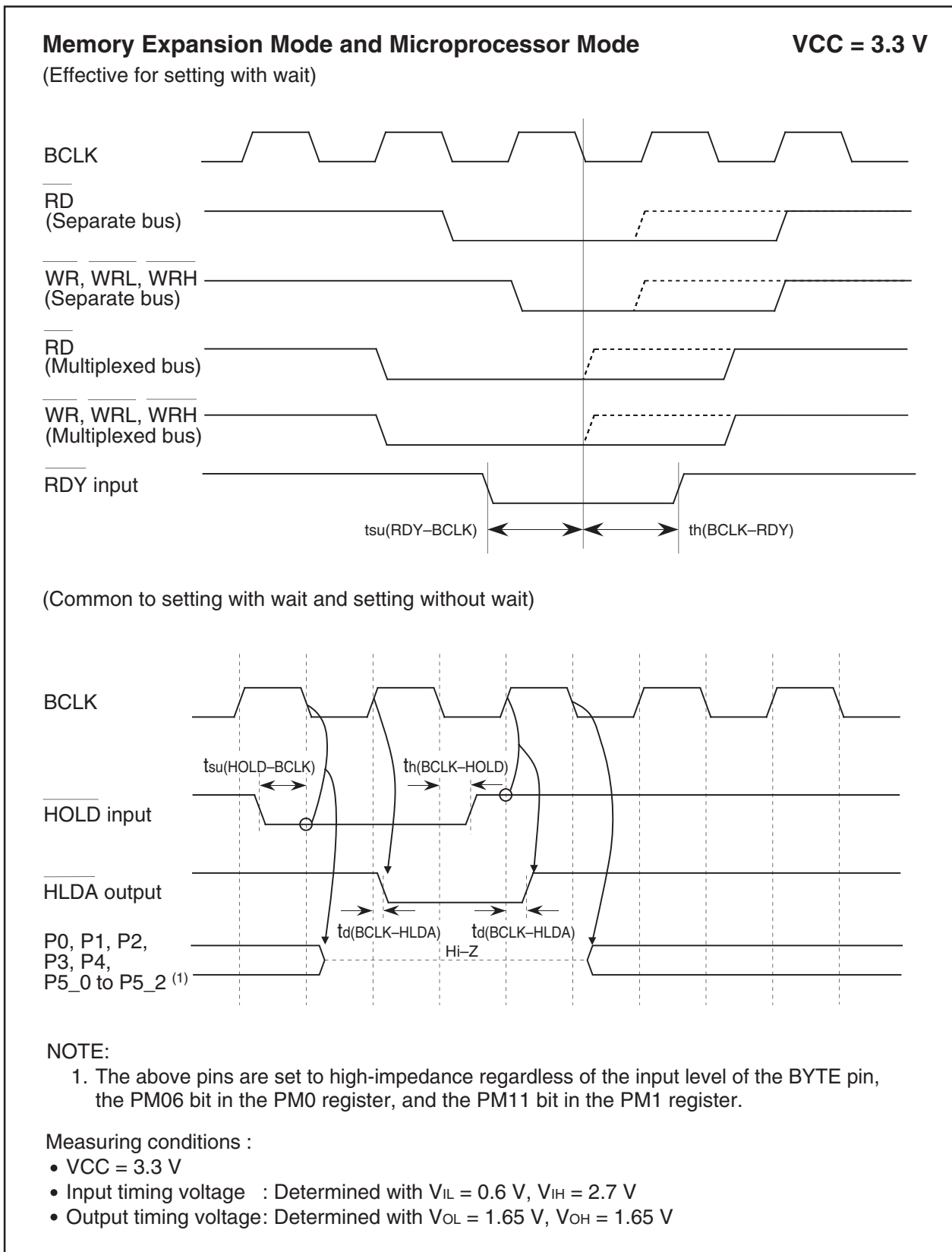


Figure 5.23 Timing Diagram (2)

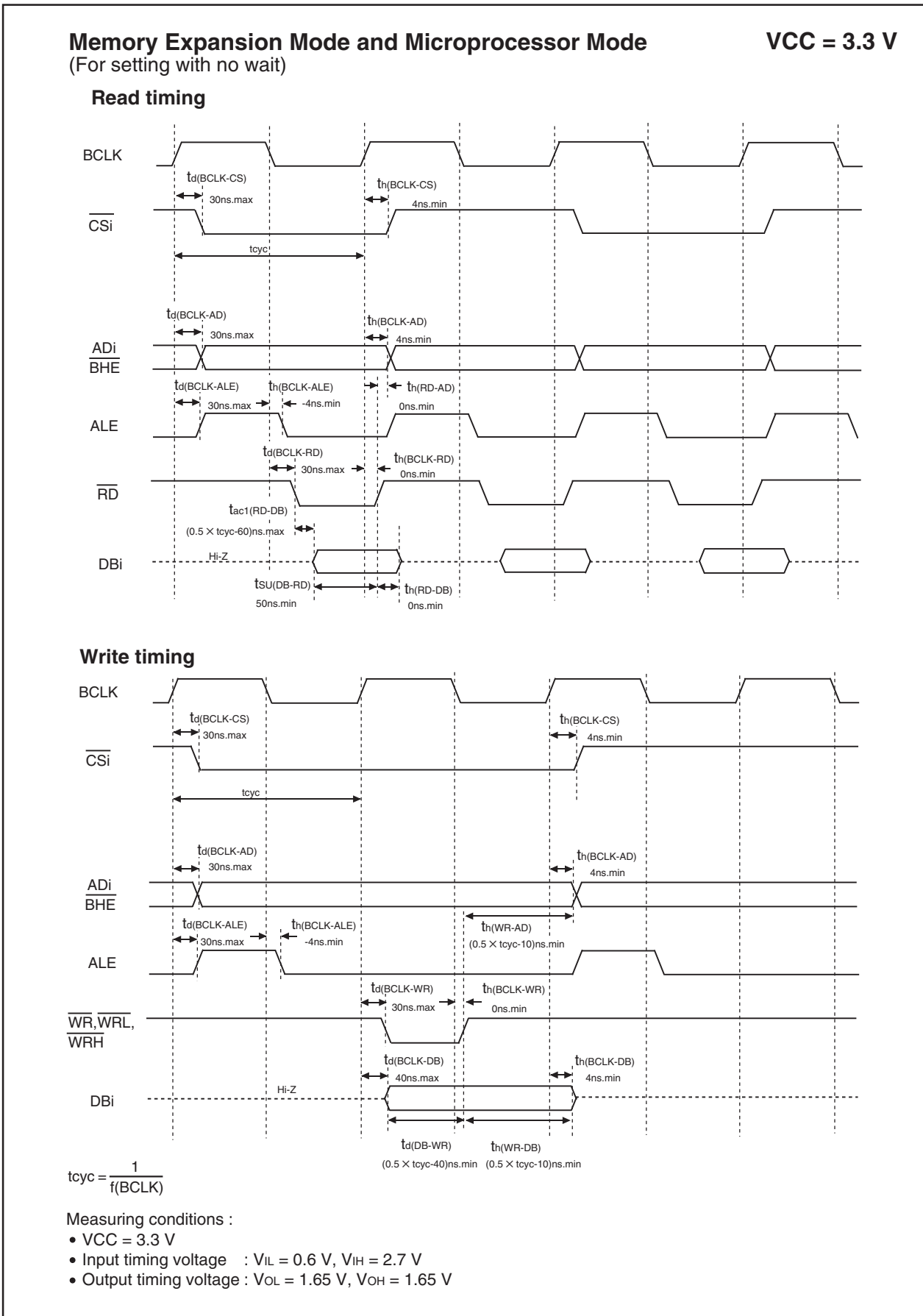


Figure 5.24 Timing Diagram (3)

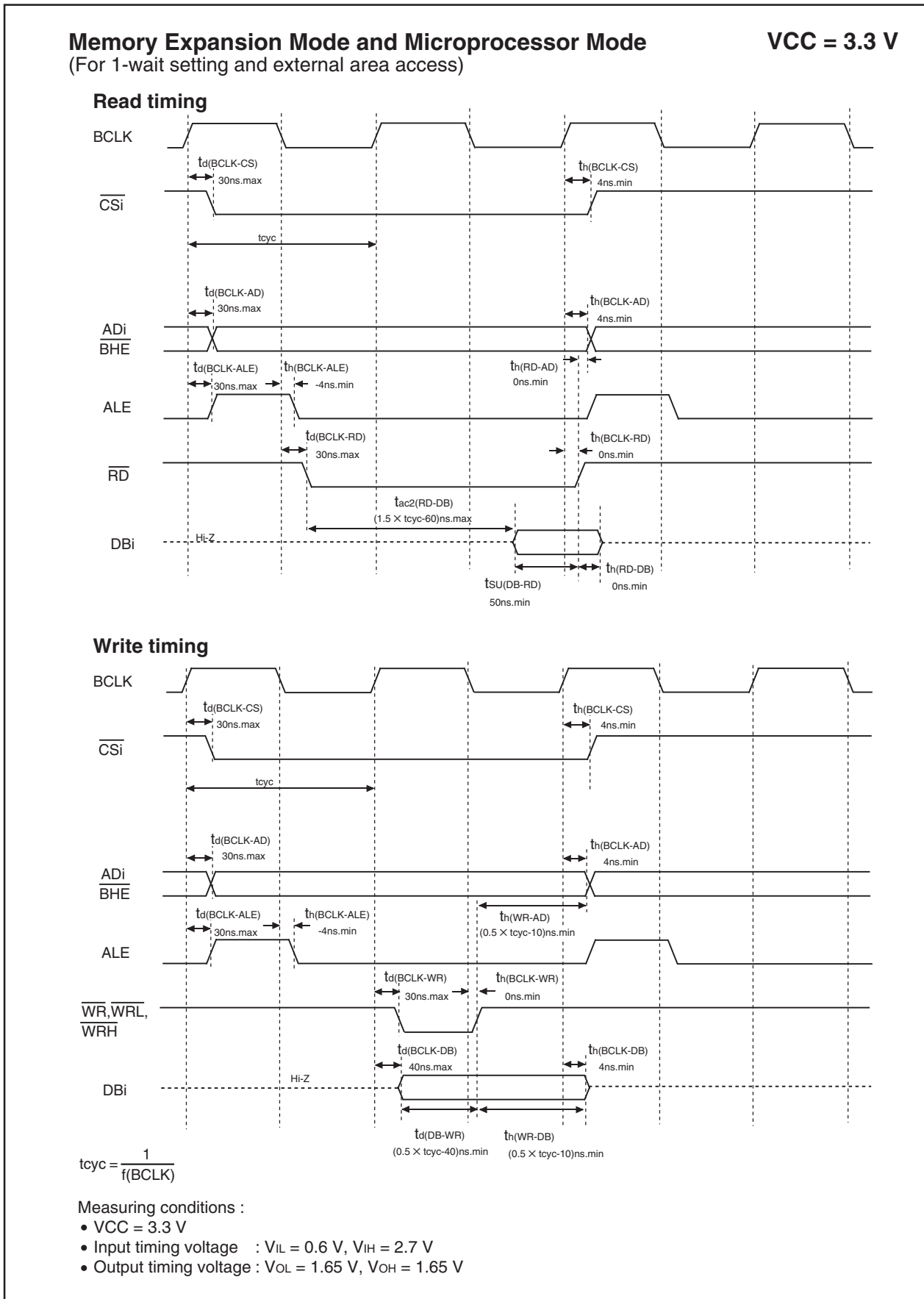


Figure 5.25 Timing Diagram (4)

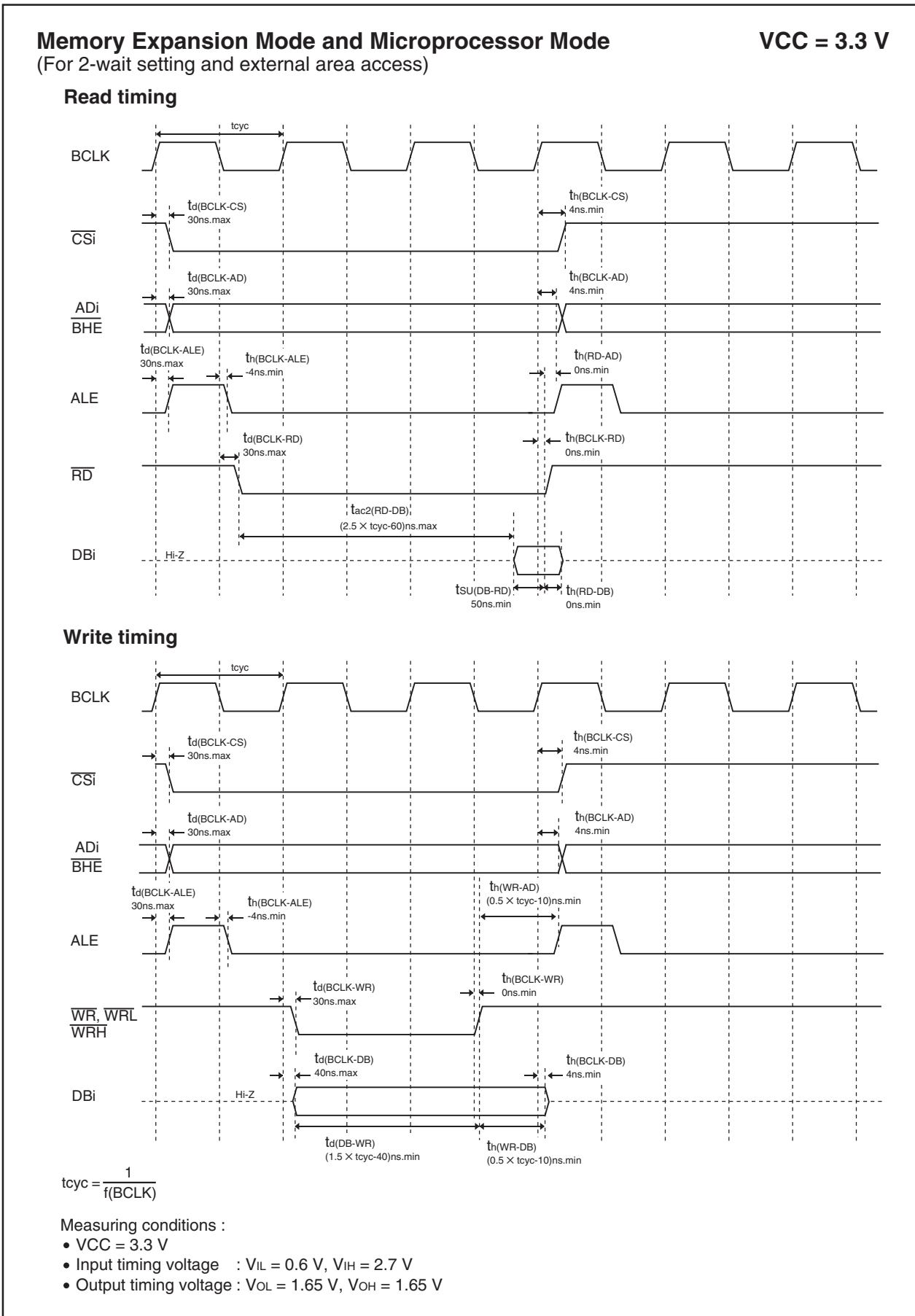


Figure 5.26 Timing Diagram (5)

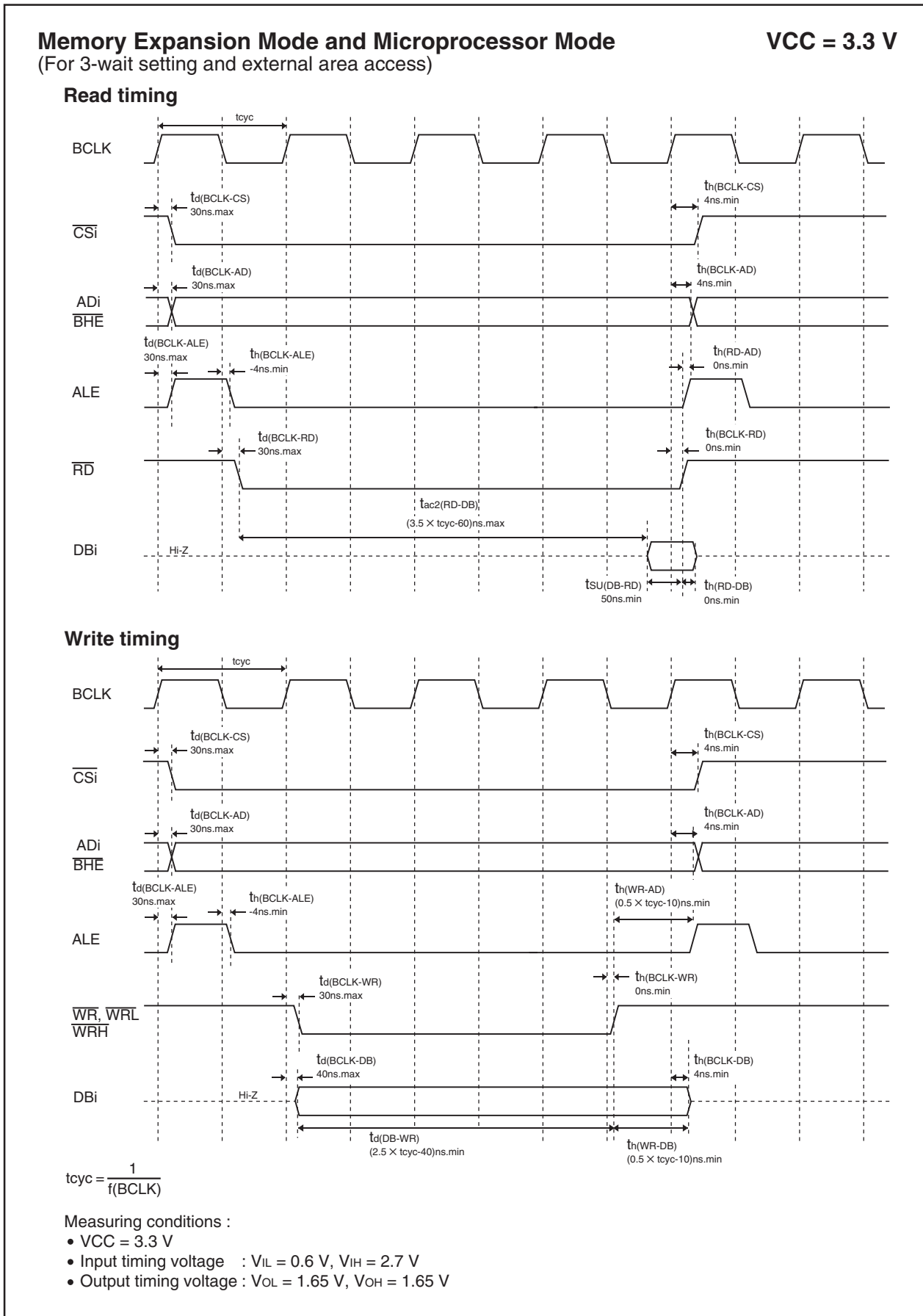


Figure 5.27 Timing Diagram (6)

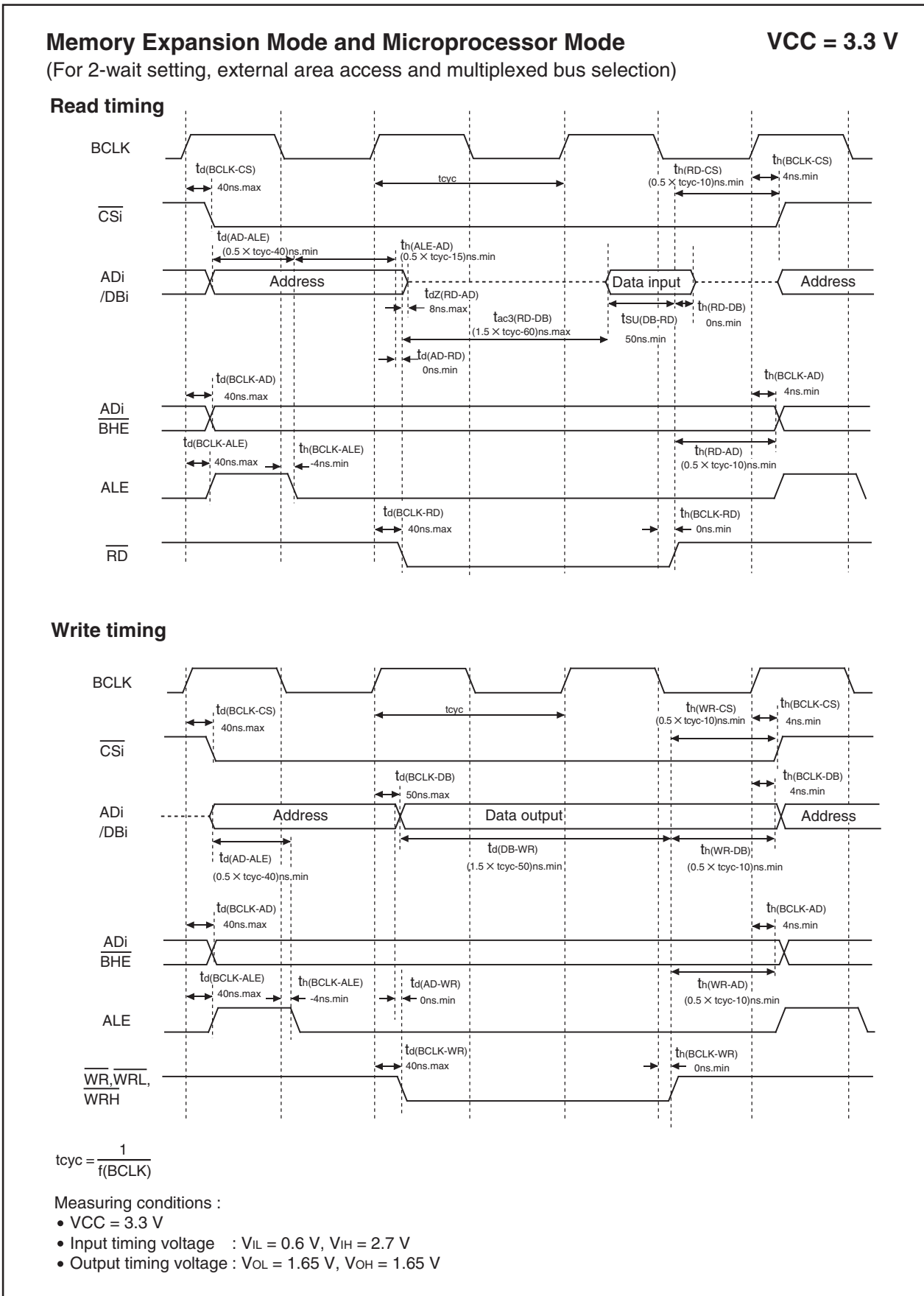


Figure 5.28 Timing Diagram (7)

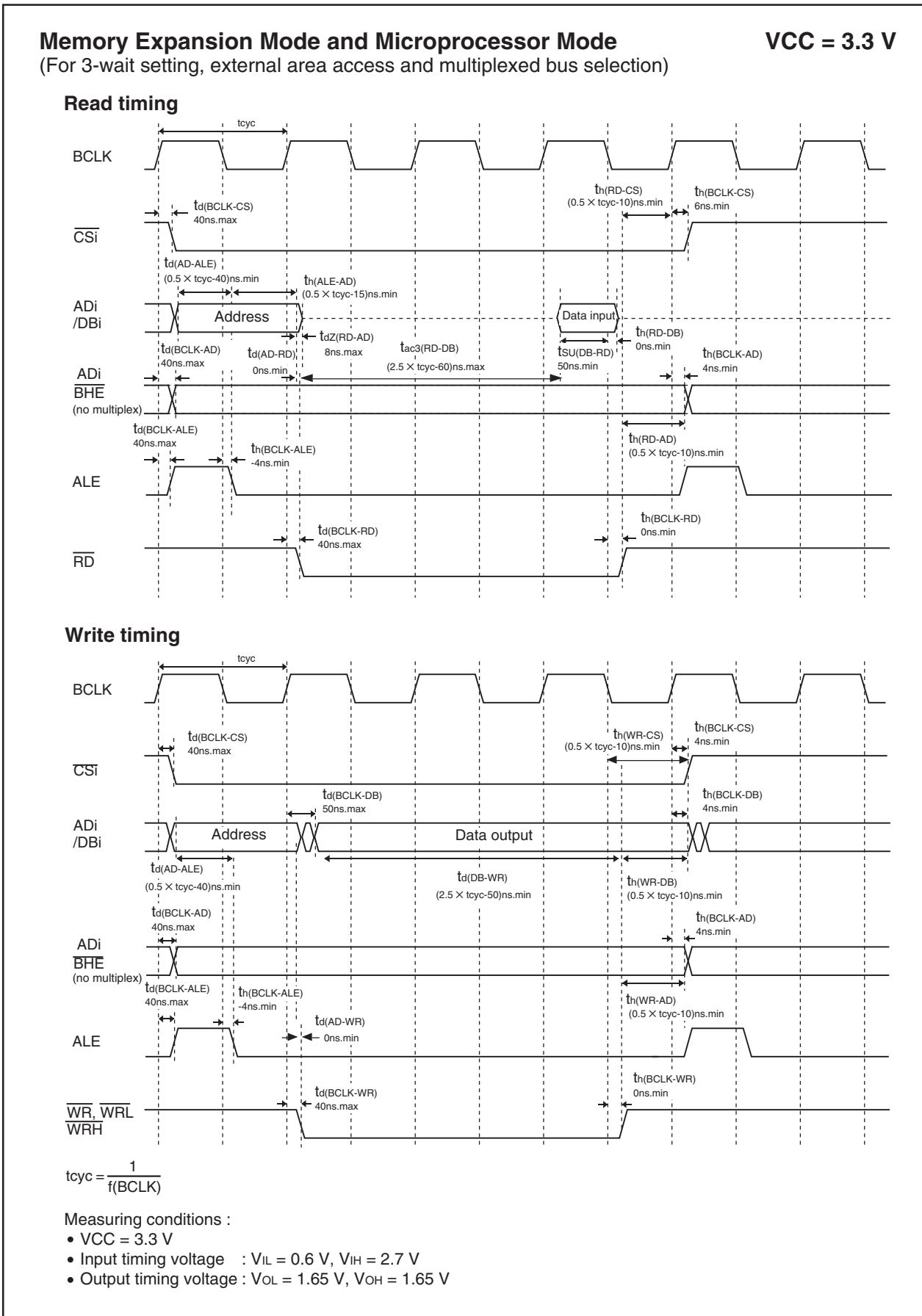
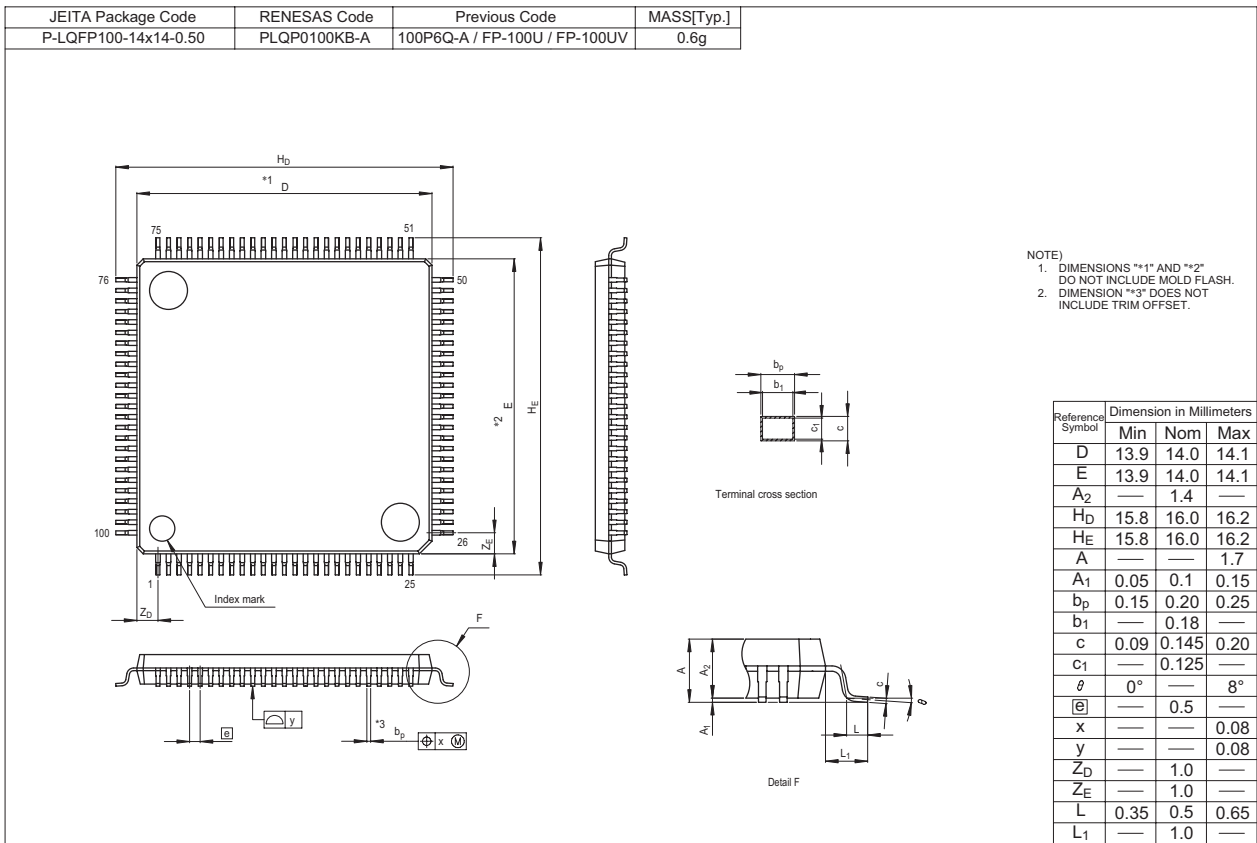
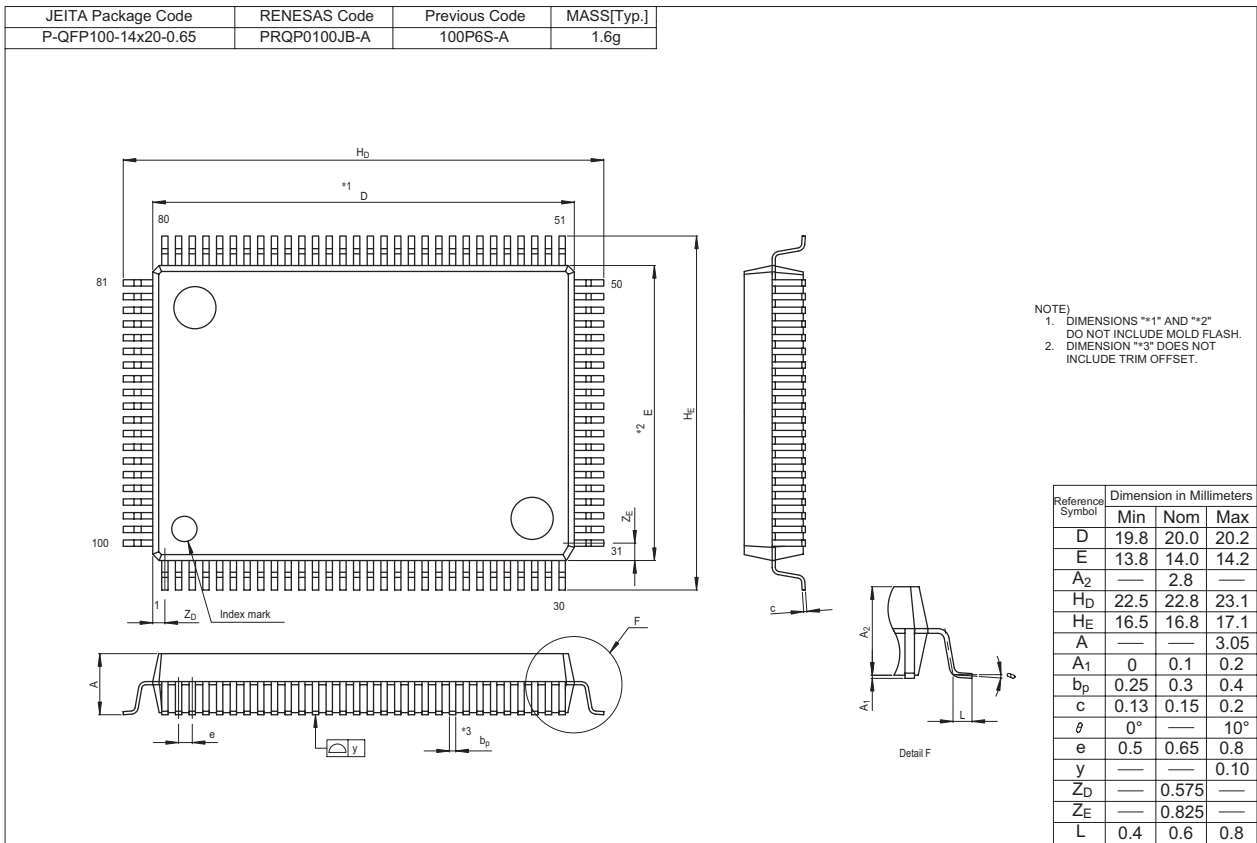


Figure 5.29 Timing Diagram (8)

Appendix 1. Package Dimensions



REVISION HISTORY

M16C/6N Group (M16C/6N4) Data Sheet

| Rev. | Date | Description | |
|------|---------------|-------------|---|
| | | Page | Summary |
| 1.00 | Jun. 30, 2003 | – | First edition issued |
| 2.00 | Nov. 10, 2004 | – | Revised edition issued * Words standardizes (on-chip oscillator) * 100P6Q-A (100-pin version) is added. * Revised parts and revised contents are as follows (except for change of a layout and an expressional change). |
| | | 1 | 1. Overview 3rd line: "and LQFP" is added. |
| | | 2 | Table 1.1 Performance outline of M16C/6N Group (M16C/6N4) • Operation Mode is added. • Address Space is added. • Power Consumption is revised. • "LQFP" is added to Package. |
| | | 4 | Table 1.2 Product List is revised. Figure 1.2 Type No., Memory Size, and Package: • "GP: Package 100P6Q-A" is added to Package type. |
| | | 5 | Figure 1.3 Pin Configuration (Top View) (1): "ZP" is added. |
| | | 6 | Figure 1.4 Pin Configuration (Top View) (2) is added. (100P6Q-A) |
| | | 8 | Table 1.4 Pin Description (2): "ZP" is added to Timer A. |
| | | 12 | 3. Memory • 5th to 6th lines: The description about the flash memory version (block A) is added. Figure 3.1 Memory Map • Interenal ROM (data area) is added. • NOTES 3, 4 are added and NOTE 5 is revised. |
| | | 13 | Table 4.1 SFR Information (1) • The value of After Reset in PM1 register is revised. • The value of After Reset in CM2 register is revised. |
| | | 19 | Table 4.7 SFR Information (7) • The value of After Reset in FMR0 register is revised. |
| | | 27 | Table 4.15 SFR Information (15) • The value of After Reset in U0C1 register is revised. • The value of After Reset in U1C1 register is revised. • NOTE 1 is added. |
| | | 28 | Table 4.16 SFR Information (16) • The value of After Reset in DA0, DA1 registers are revised. |
| | | 29 | Table 5.1 Absolute Maximum Ratings • "Flash Program Erase" in Operating Ambient Temperature is added. |
| | | 31 | Table 5.3 Recommended Operating Conditions (2) • Parameters of Power Supply Ripple are added. • NOTE 4 is revised. Figure 5.1 Timing of Voltage Fluctuation is added. |
| | | 32 | Table 5.4 Electrical Characteristics (1): Hysteresis • "CLK4" is revised to "CLK3", and "TA2OUT" is revised to "TA0OUT". • Max. of Standard in $\overline{\text{RESET}}$ is revised from "2.2" to "2.5". • XIN is added. |

REVISION HISTORY

M16C/6N Group (M16C/6N4) Data Sheet

| Rev. | Date | Description | |
|------|--|-------------|---|
| | | Page | Summary |
| 2.00 | Nov. 10, 2004 | 34 | Table 5.6 A/D Conversion Characteristics: "Tolerance Level Impedance" is added. |
| | | 35 | Table 5.8 Power Supply Circuit Timing Characteristics: " $t_{d(M-L)}$ " is deleted. Figure 5.2 Power Supply Circuit Timing Diagram is added. |
| | | 36 | Table 5.10 Memory Expansion Mode and Microprocessor Mode: " $t_{d(BCLK-HLDA)}$ " is deleted. |
| | | 38 | Table 5.21 Serial I/O: Min. of standard in $t_{su(D-C)}$ is revised from "30" to "70". |
| | | 39 | Table 5.23 Memory Expansion Mode and Microprocessor Mode (for setting with no wait) <ul style="list-style-type: none"> • Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15". • $t_{d(BCLK-HLDA)}$ is added. |
| | | 40 | Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access) <ul style="list-style-type: none"> • Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15". • $t_{d(BCLK-HLDA)}$ is added. |
| | | 41 | Table 5.25 Memory Expansion Mode and Microprocessor Mode (for 2- to 3-wait setting, external area access and multiplexed bus selection) <ul style="list-style-type: none"> • $t_{d(BCLK-HLDA)}$ is added. • Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15". |
| | | 42 | Figure 5.4 Timing Diagram (1): "XIN input" is added. |
| | | 44, 45 | Figures 5.6 and 5.7 Timing Diagram (3) (4): "DB" in Read timing is revised to "DBi". |
| | | 46, 47 | Figures 5.8 and 5.9 Timing Diagram (5) (6): "DB" in Write timing is revised to "DBi". |
| | | 49 | Figure 5.11 Timing Diagram (8) <ul style="list-style-type: none"> • "ADi/DB" in Read/Write timing is revised to "ADi/DBi". |
| | | 50 | Appendix 1. Package Dimensions: 100P6Q-A is added. |
| | | 2.10 | Jun. 24, 2005 |
| 2 | Table 1.1 Performance outline of M16C/6N Group (M16C/6N4) <ul style="list-style-type: none"> • Performance outline of Normal-ver. is added. | | |
| 4 | Table 1.2 Product List is revised. (Normal-ver. is added.) Figure 1.2 Type No., Memory Size, and Package: <ul style="list-style-type: none"> • "(no): Normal-ver." is added to Characteristics. | | |
| 19 | Figure 4.7 SFR Information (7): NOTE 1 is revised. | | |
| 32 | Table 5.4 Electrical Characteristics (1) <ul style="list-style-type: none"> • Measuring Condition of V_{OL} is revised from "$L_{OL} = -200\mu A$" to "$L_{OL} = 200\mu A$". | | |
| 33 | Table 5.5 Electrical Characteristics (2): Mask ROM (5th item) <ul style="list-style-type: none"> • "$f(XCIN)$" is changed to "$f(BCLK)$". | | |
| 34 | Table 5.6 A/D Conversion Characteristics: "Tolerance Level Impedance" is deleted. | | |
| 2.40 | Aug. 25, 2006 | – | Revised edition issued * Electric Characteristics of Normal-ver. is added. * Revised parts and revised contents are as follows (except for expressional change). |
| | | 1 | 1.1 Applications: Comment of Normal-ver. is added. |
| | | 4 | Table 1.2 Product Information <ul style="list-style-type: none"> • Status of development is revised and NOTES 1 and 2 are added. |

REVISION HISTORY

M16C/6N Group (M16C/6N4) Data Sheet

| Rev. | Date | Description | |
|------|---------------|---|---|
| | | Page | Summary |
| 2.40 | Aug. 25, 2006 | 7, 8 9 22 33 34 52 to 87 | <p>Tables 1.3 and 1.4 List of Pin Names (1)(2) are added.</p> <p>Table 1.5 Pin Functions (1)</p> <ul style="list-style-type: none"> • 3.0 to 5.5 V (Normal-ver.) is added to Description of Power supply input. <p>Table 4.8 SFR Information (8)</p> <ul style="list-style-type: none"> • The value of After Reset in IDB0 register is revised. • The value of After Reset in IDB1 register is revised. <p>Table 5.3 Recommended Operating Conditions (2)</p> <ul style="list-style-type: none"> • Power supply ripple is deleted. (three items) <p>Figure 5.1 Voltage Fluctuation Timing is deleted.</p> <p>Table 5.4 Electrical Characteristics (1): Hysteresis XIN is deleted.</p> <p>5.2 Electrical Characteristics (Normal-ver.) is added.</p> |
| | | | |

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